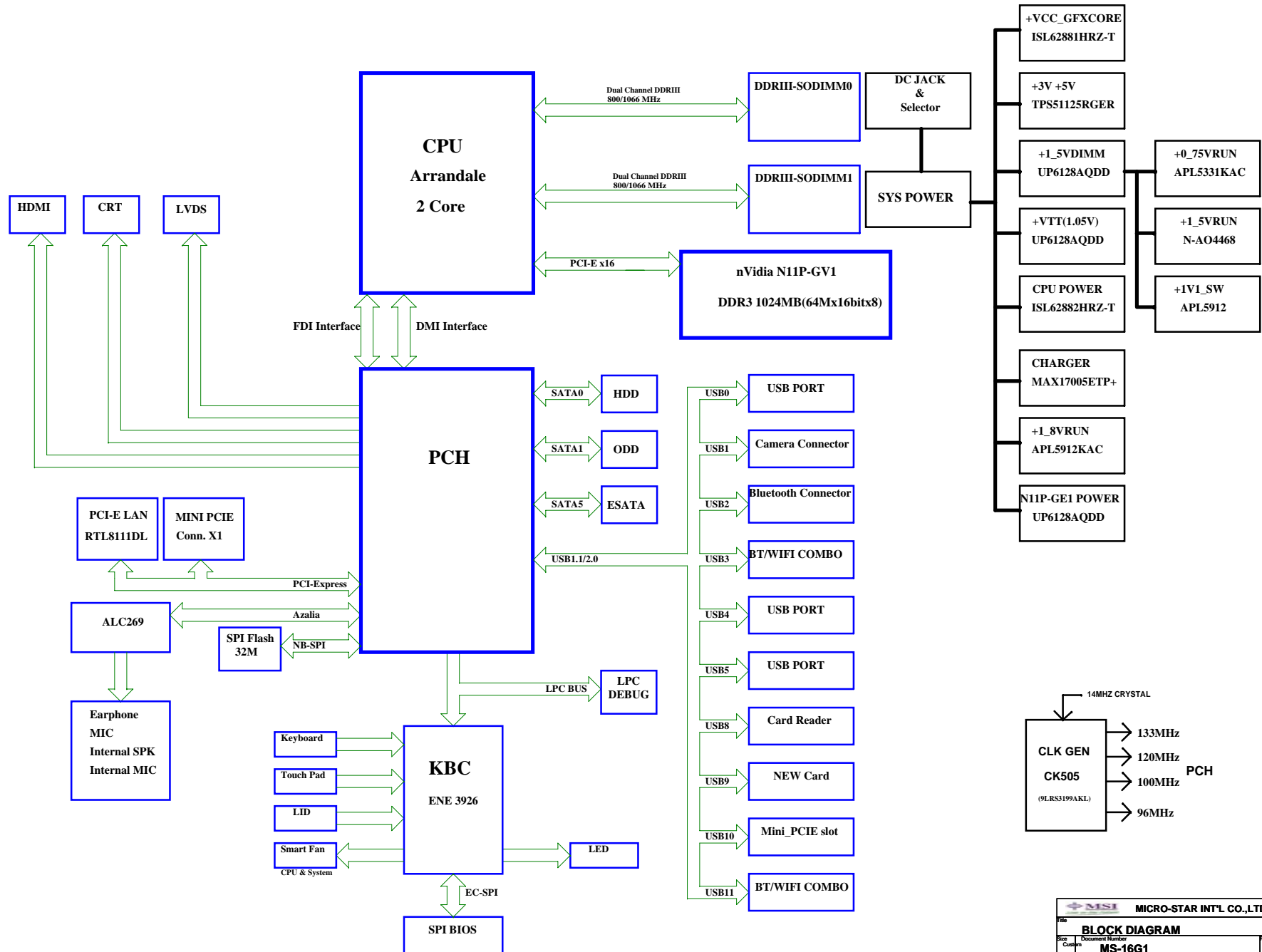


Calpella Platform

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28 :	PCH-9 (GND)
29 :	Clock Generator (9LRS3199AKL)
30 :	KBC/EC/uP (KB3926)
31 :	PCIE 10/100/1000 LAN (RTL8111DL)
32 :	Cardreader (UB6250)
33 :	FAN,Launch board
34 :	HDD,CDROM,USB,NEWCARD,ESATA
35 :	MINIPICIE,CAMERA,BLUETOOTH,SW
36 :	CODEC(ALC662)&Amp
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38 :	M_Battery select
39 :	M_Battery Charger
40 :	M_System Power
41 :	SMDDR_VTERM/1_5VRUN
42 :	VTT POWER,+1.8VRUN
43 :	M_CPU power
44 :	M_Graphic Core
45 :	M92/Park power
46 :	SCREW/ME
47 :	88A USB BOARD
48 :	88B_Touch Pad Board
49 :	EMI
50 :	Power ON Sequency
51 :	Power Down Sequence
52 :	Power MAP



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

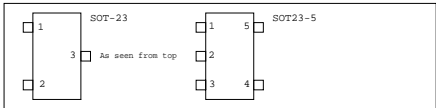
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
M92S_VDD_CORE	0.95V	S0	GPU core power
+1_8VRUN_PARK	1.8V	S0	GPU PCIE power
+1_5VRUN_PARK	1.5V	S0	GPU DDR3 power
+1_0VRUN_PARK	1.0V	S0	GPU PCIE power
VDDR3	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

Suffix
L = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

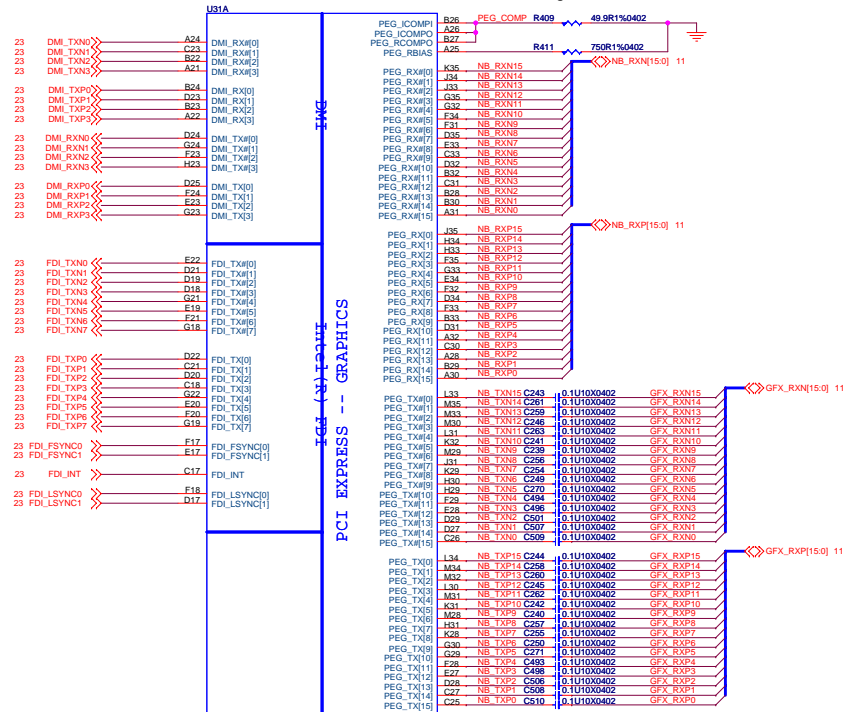
Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)

10 mils trace wide
20 mils trace space
500 mils trace length



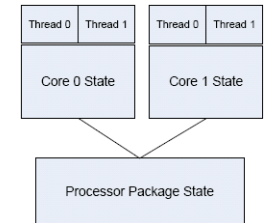
N12-9880010-L06
PGA980
IC_AUB_CFD_PGA_R0P9

Westmere (formerly Nehalem-C) is the name given to the 32 nm die shrink of Nehalem.

Brand Name	Model (list)	L3 Cache size	Thermal Design Power
Intel Core i3	i3-3xxM	3 MB	35 W
Intel Core i5	i5-4xxM	3 MB	35 W
	i5-5xxM	3 MB	35 W
Intel Core i7	i7-6xxUM	4 MB	18 W
	i7-6xxLM	4 MB	25 W
	i7-6xxM	4 MB	35 W

The Core i3-3xx will be similar to the Core i5-4xx series but running at lower clock speeds and without Turbo Boost

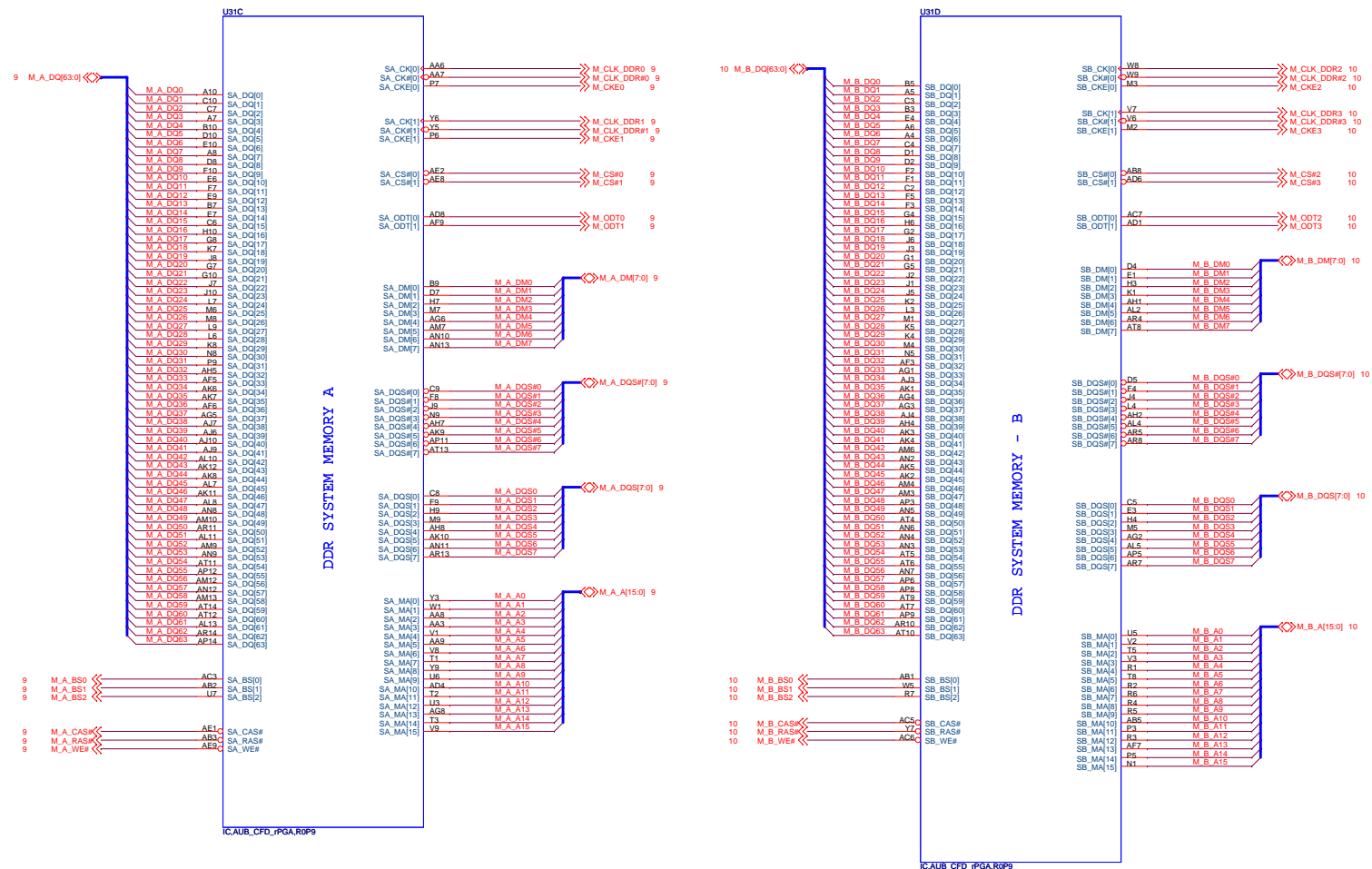
Brand	Intel Core i3	Intel Core i5	Intel Core i7	Intel Core i9	Intel Core i11	Intel Core i12	Intel Core i13
Segment	POP1	POP2	POP3	ULV1	ULV2	LV1	LV2
TDP	35W	35W	35W	18W	18W	25W	25W
Cores/Threads	2/4	2/4	2/4	2/4	2/4	2/4	2/4
CPU Base Freq (GHz)	2.40	2.53	2.66	1.06	1.2	2.00	2.13
Intel® Turbo Boost Technology Max 9C Turbo (GHz)	2.93	3.06	3.33	2.13	2.26	2.80	2.93
DDR3 (MHz)	1066MHz	1066MHz	1066MHz	800MHz	800MHz	1066MHz	1066MHz
L3 Cache	3MB	3MB	4MB	4MB	4MB	4MB	4MB
Integrated Gfx	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Gfx Base Render Frequency	500MHz	500MHz	500MHz	166MHz	166MHz	266MHz	266MHz
Intel® Turbo Boost Technology Max Gfx Render (MHz)	766MHz	766MHz	766MHz	500MHz	500MHz	566MHz	566MHz
Intel® Hyper-threading /VT/TXT/Intel® vPro	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package	BGA/PGA	BGA/PGA	BGA/PGA	BGA	BGA	BGA	BGA

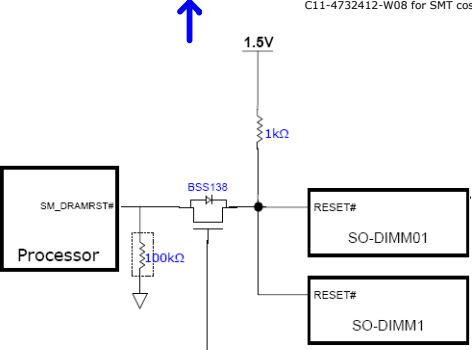
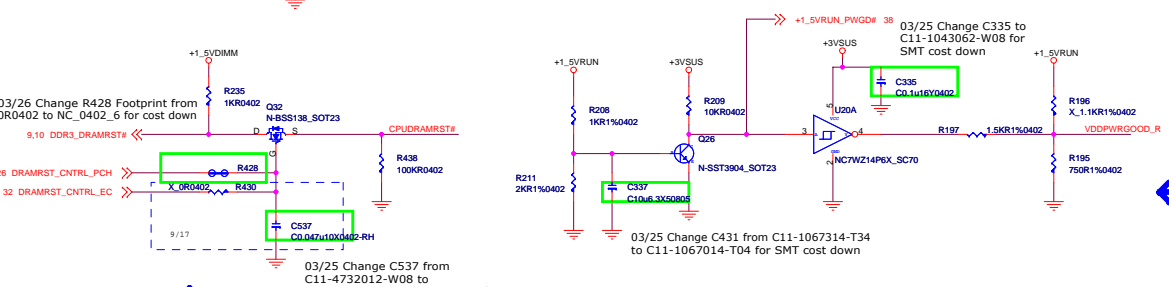
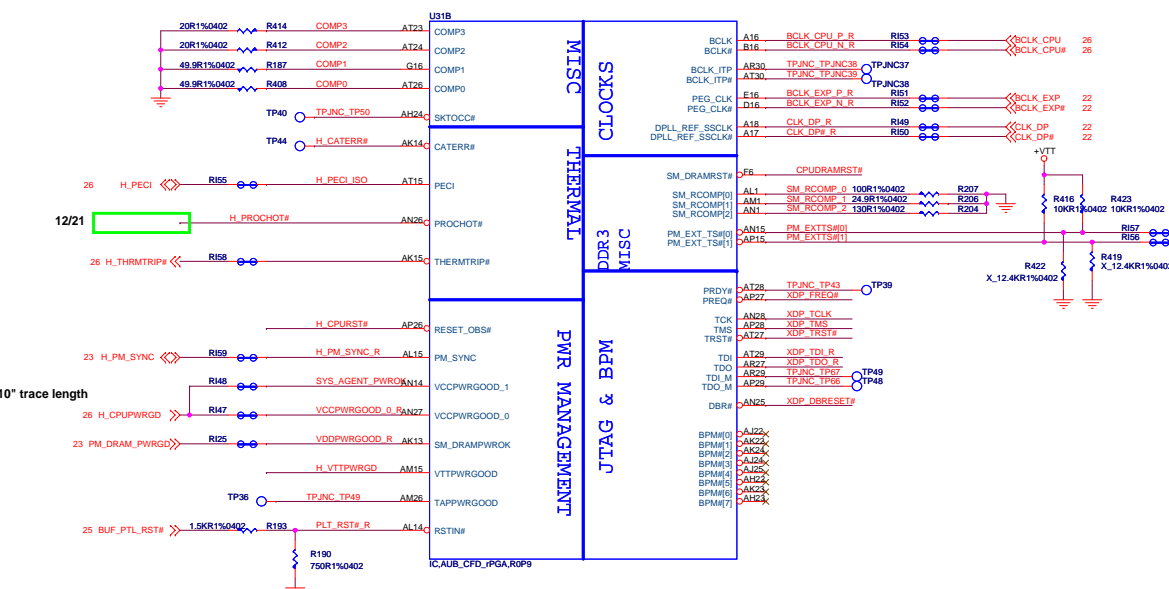


Coordination of Thread Power States at the Core Level

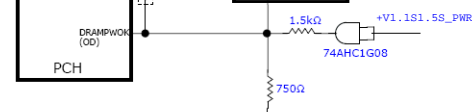
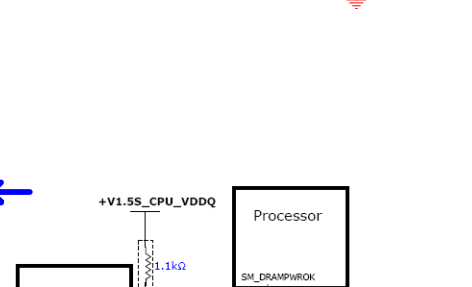
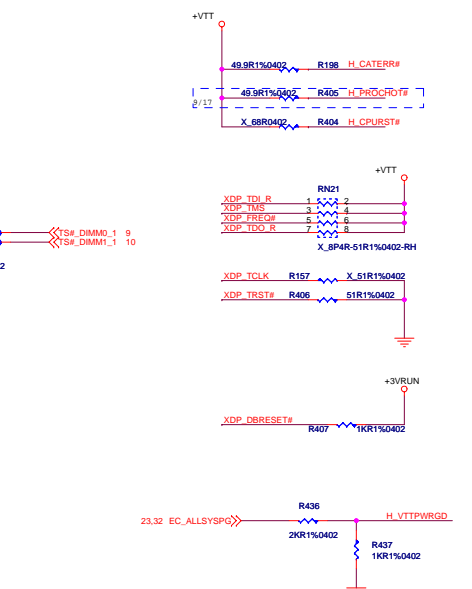
Processor Core C-State		Thread 1			
Thread 0	C0	C0	C1	C3	C6
	C1	C0	C1 ¹	C1 ¹	C1 ¹
	C3	C0	C1 ¹	C3	C3
	C6	C0	C1 ¹	C3	C6

ARRANDALE PROCESSOR (DDR3)





When Processor V_{DDQ} power is turned off in S3, SM_DRAMRST# will also go low with processor power. To avoid SM_DRAMRST# going low, a FET (e.g., BSS138) is added which is controlled using a PCH GPIO (RST_GATE). A Pull-up resistor of 1 k Ω to +1.5V_DIMM is added at SM_DRAMRST#_pin of SO-DIMM. Before system enters S3 (Before SLP_S3# going low), RST_GATE is driven low and FET is turned off. With a 1-k Ω PU on the SO-DIMM side, SM_DRAMRST# is maintained high during S3. When exiting S3, the FET will remain off until the integrated memory controller is reinitialized to drive the SM_DRAMRST# signal to a high level after the Processor V_{DDQ} power is restored.



SM_DRAMPWROK signal is driven low when PROCESSOR is turned off in S3 entry. During S3 exit, this signal is driven high only after +V1.5S_CPU_VDDQ stable. There is no timing requirement between and 0.75-V V_{TT} rail.

+V1.5S_PWRGD signal is an open-drain signal driven from +V1.5S_CPU_VDDQ PWRGOOD logic. It should go high only after +V1.5S_CPU_VDDQ to processor is stable.

DRAMPWROK behavior in S5/S4 to S0:

During S5/S4 to S0, DRAMPWROK is driven low by PCH until PCH_PWROK becomes high provided SLP_S4# is high. Even though DRAMPWROK derived from PWRGOOD of +V1.5S_CPU_VDDQ comparator, it is overdriven to low by PCH until PCH_PWROK goes high. This implementation ensures that S5 to S0 timings are maintained.

DRAMPWROK behavior in S0 to S3:

This signal is driven low as the +V1.5S_PWRGD becomes low when +V1.5S_CPU_VDDQ ramps down. To maintain this signal low, this AND gate is powered using SUS rail (+V3.3A). Any buffer/AND gate of 4 mA should work fine in the given circuit.

DRAMPWROK behavior in S3 to S0:

This signal is driven high when +V1.5S_CPU_VDDQ to the processor is stable DRAMPWROK is 1.1-V/1.05-V signal to processor; hence a resistor divider is implemented to level translate the signal.

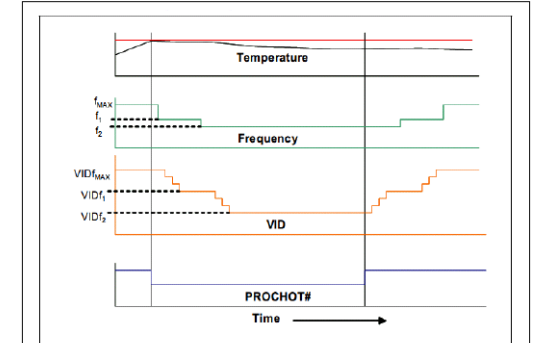
Refer to the latest Intel CRB schematics for more details on +V1.5S_PWRGD generation.

Arrandale Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
BCLK/BCLK#	133 MHz	Processor/Memory/Graphics
PEG_CLK/PEG_CLK#	100 MHz	PCI Express/DMI/Intel® FDI
DPPLL_REF_SSCLK/DPPLL_REF_SSCLK#	120 MHz	Embedded DisplayPort (eDP)

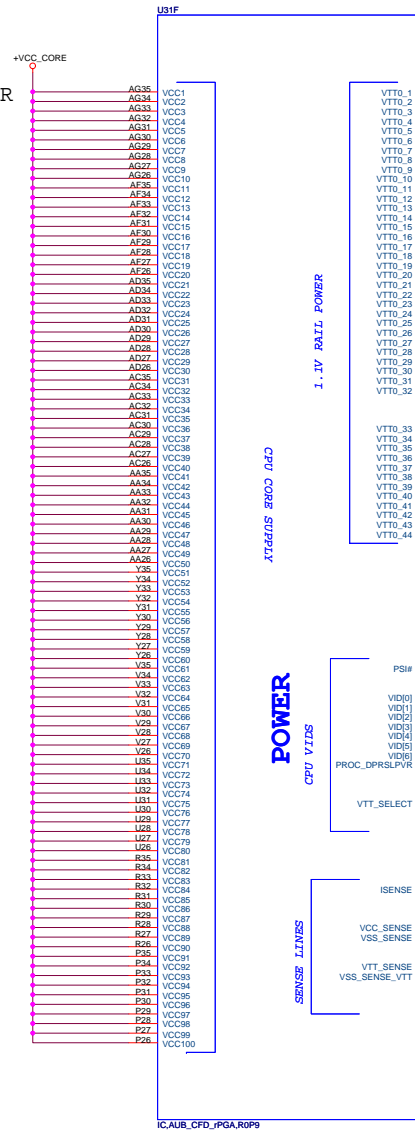
Signal Name	Description	Direction/Buffer Type
VCCPWRGOOD_0 VCCPWRGOOD_1	VCCPWRGOOD_0 and VCCPWRGOOD_1 (Power Good) Processor Input: The processor requires these signals to be a clean indication that: -VCC, VCCPLL, and VTT supplies are stable and within their specifications -BCLK is stable and has been running for a minimum number of cycles. Both signals must then transition monotonically to a high state. VCCPWRGOOD_0 and VCCPWRGOOD_1 can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of these signals. VCCPWRGOOD_0 and VCCPWRGOOD_1 should be tied together and connected to the PROCPWRGD output signal of the PCH.	I Asynchronous CMOS

Frequency and Voltage Ordering

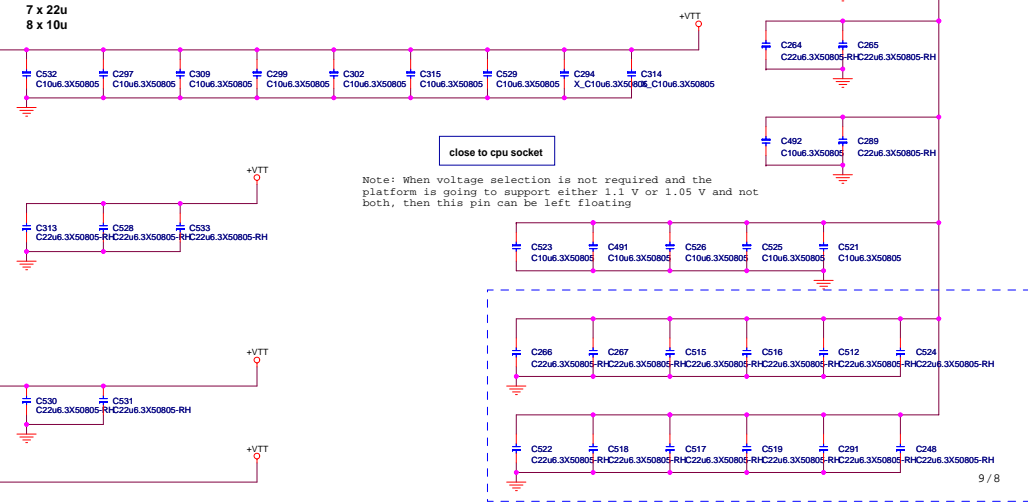


ARRANDALE:
SV=48A
LV=35A
ULV=27A

+VCC_CORE



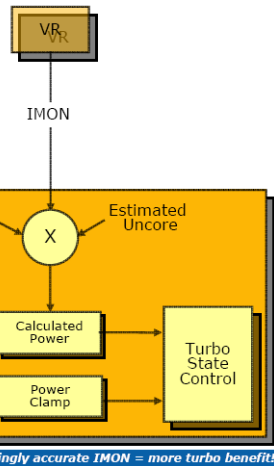
ARRANDALE :
SV=18A
LV=TBD
ULV=TBD



close to cpu socket

Symbol	Parameter	Min	Typ	Max	Unit
V _{TT}	Voltage for the memory controller and shared cache defined at the motherboard VTT pinfield via	0.9975	1.05	1.1025	V
	Voltage for the memory controller and shared cache defined across VTT_SENSE and VSS_SENSE_VTT	0.9765	1.05	1.1235	V
V _{DDQ} (DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	1.425	1.5	1.575	V
V _{CCPLL}	PLL supply voltage (DC + AC specification)	1.710	1.8	1.890	V
I _{CCMAX_VTT}	Max Current for V _{TT} Rail SV LV ULV		-	18 16 16	A
I _{CCMAX_VDDQ}	Max Current for V _{DDQ} Rail		-	3	A
I _{CCMAX_VDDQ_OK}	BGA Only.			0.2	A
I _{CCMAX_VTTO_DDR}	BGA Only			2.6	A
I _{CCMAX_VCCPLL}	Max Current for V _{CCPLL} Rail		-	1.35	A
I _{CTDC_VTT}	Thermal Design Current (TDC) for V _{TT} Rail SV LV ULV		-	18 16 16	A
I _{CAVG_VDDQ} (Standby)	Average Current for V _{DDQ} Rail during Standby		-	0.33	A

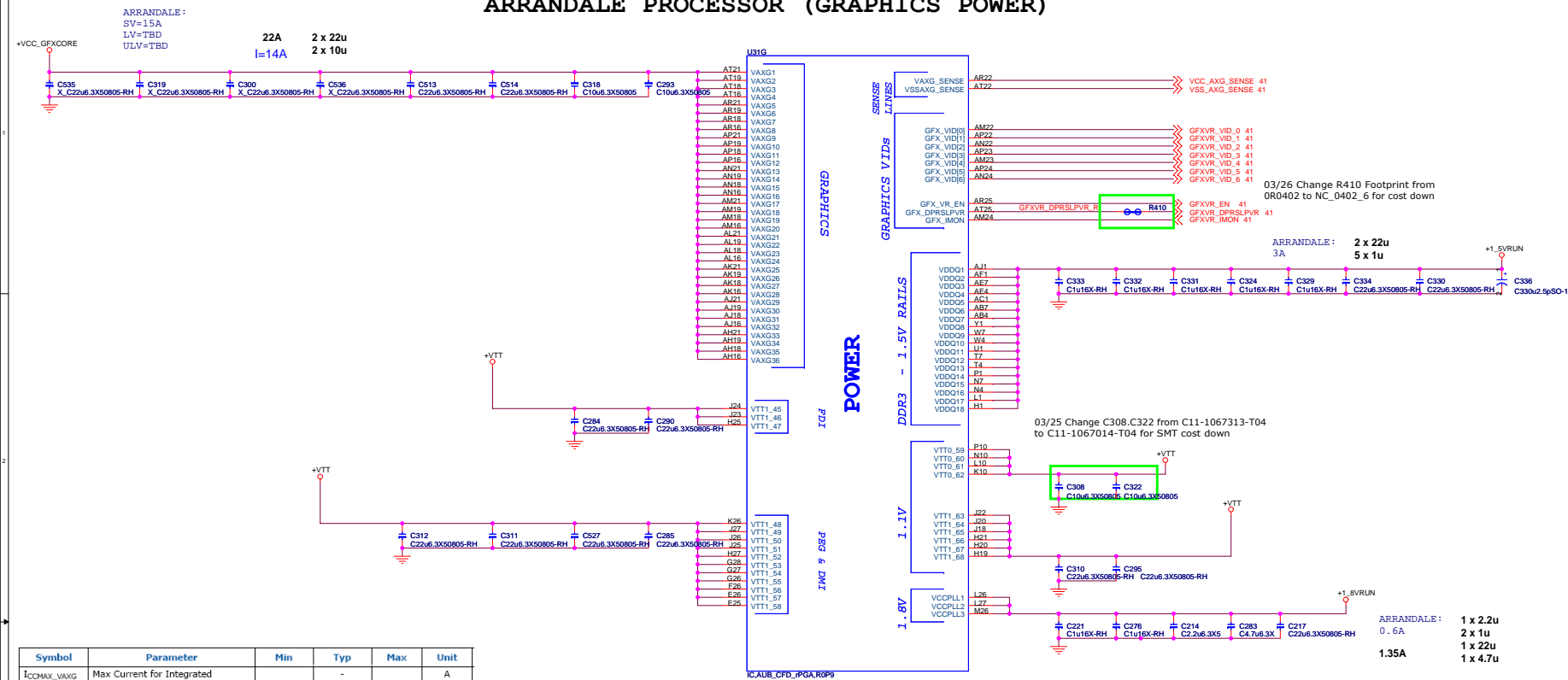
Symbol	Parameter	Segment	Min	Typ	Max	Unit
I_{CCMAX}	Maximum Processor Core I_{CC}	SV LV ULV		48 35 27		A
I_{CC_TDC}	Thermal Design I_{CC}	SV LV ULV		32 22 16		A
I_{CC_LPM}	I_{CC} at LPM	SV LV ULV		18 12 8		A
I_{C6}	I_{CC} at C6 Idle-state	SV LV ULV			0.3 0.3 0.3	A



CPU SKU, I _{CC_CORE-MAX} Maximum CPU Core Current	I _{MAX} (1M000 mV [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled		000	
I _{CC_CORE-MAX} ≤ 20 A	20	001	45.0
20A < I _{CC_CORE-MAX} ≤ 30 A	30	010	30.0
30A < I _{CC_CORE-MAX} ≤ 40 A	40	011	22.5
40A < I _{CC_CORE-MAX} ≤ 50 A	50	100	18.0
50A < I _{CC_CORE-MAX} ≤ 60 A	60	101	15.0
60A < I _{CC_CORE-MAX} ≤ 70 A	70	110	12.0
70A < I _{CC_CORE-MAX} ≤ 90 A	90	111	10.0

MSID[2]	MSID[1]	MSID[0]	Description ^{1,2}
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Arrandale Standard Voltage (SV) 35W Supported
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

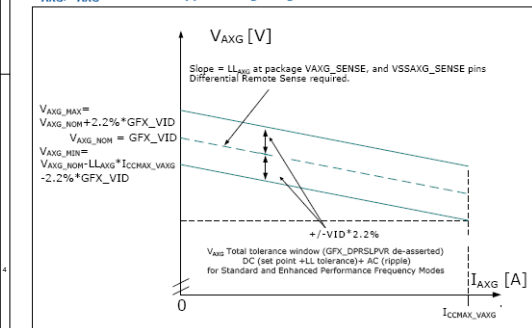
ARRANDALE PROCESSOR (GRAPHICS POWER)



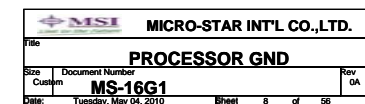
Symbol	Parameter	Min	Typ	Max	Unit
I _{CCMAX_VAUX}	Max Current for Integrated Graphics Rail SV LV ULV		-	22 15 12	A
I _{CCTDC_VAUX}	Thermal Design Current (TDC) for Integrated Graphics Rail SV LV ULV		-	12 7 6	A

Symbol	Parameter	Min	Typ	Max	Unit
V _{AXG}	Graphics core voltage	See Figure 15			

V_{AXG}/I_{AXG} Static and Ripple Voltage Regulation



ARRANDALE PROCESSOR (RESERVED)



SODIMM#A

4 M.A. A[15:0] >>> M.A. A0 98 A0
M.A. A1 97 A1
M.A. A2 96 A2
M.A. A3 95 A3
M.A. A4 92 A4
M.A. A5 91 A5
M.A. A6 90 A6
M.A. A7 86 A7
M.A. A8 89 A8
M.A. A9 85 A9
M.A. A10 107 A10/A9
M.A. A11 84 A11
M.A. A12 83 A12
M.A. A13 119 A13
M.A. A14 80 A14
M.A. A15 78 A15

4 M.A. B0 >>> 109 BA0
4 M.A. B1 >>> 108 BA1
4 M.A. B2 >>> 79 BA2
4 M.CS#0 >>> 114 CS0
4 M.CS#1 >>> 121 CS1
4 M.CLK_DDR0 >>> 101 CK0
4 M.CLK_DDR#0 >>> 103 CK#0
4 M.CLK_DDR1 >>> 102 CK1
4 M.CLK_DDR#1 >>> 104 CK#1
4 M.CKE0 >>> 74 CKE0
4 M.CKE1 >>> 73 CKE1
4 M.A. CAS# >>> 115 CAS#
4 M.A. RAS# >>> 110 RAS#
4 M.A. WE# >>> 113 WE#

SAD_DIM0 197 SA0
SD_DIM0 201 SA1
SD_DIM0 202 SCL
SD_DIM0 200 SDA

10.22.30.34 SMB_CLK_DIMM >>> R22
10.22.30.34 SMB_DATA_DIMM >>> R120

4 M_ODT0 >>> 116 ODT0
4 M_ODT1 >>> 120 ODT1

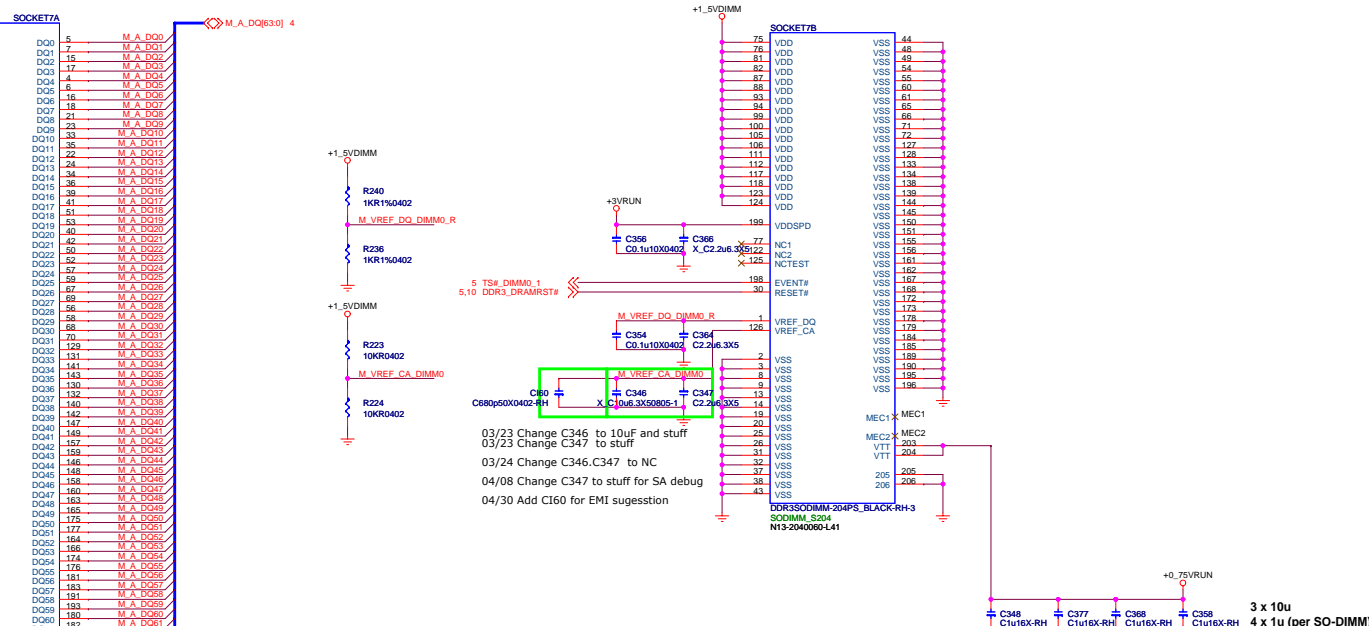
4 M.A. DM0[7:0] >>> M.A. DM0 11 DM0
M.A. DM1 28 DM1
M.A. DM2 46 DM2
M.A. DM3 63 DM3
M.A. DM4 136 DM4
M.A. DM5 153 DM5
M.A. DM6 170 DM6
M.A. DM7 167 DM7

4 M.A. DQS[7:0] >>> M.A. DQS0 12 DQS0
M.A. DQS1 28 DQS1
M.A. DQS2 47 DQS2
M.A. DQS3 64 DQS3
M.A. DQS4 137 DQS4
M.A. DQS5 154 DQS5
M.A. DQS6 171 DQS6
M.A. DQS7 188 DQS7

4 M.A. DQS#7 >>> M.A. DQS#7 10 DQS#7
M.A. DQS#0 47 DQS#0
M.A. DQS#1 62 DQS#1
M.A. DQS#2 75 DQS#2
M.A. DQS#3 135 DQS#3
M.A. DQS#4 152 DQS#4
M.A. DQS#5 169 DQS#5
M.A. DQS#6 186 DQS#6
M.A. DQS#7 186 DQS#7

SAD_DIM0 R22
SAT_DIM0 R128
DIM0 R227

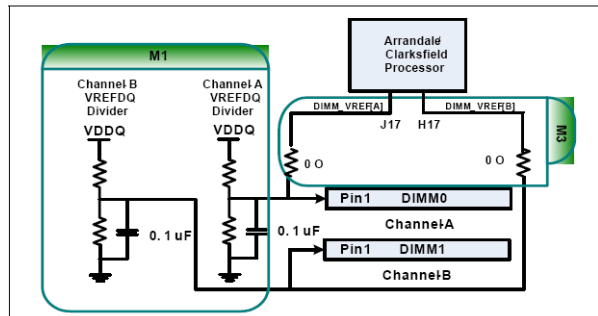
DDR3SO
SODIMM
R15-204



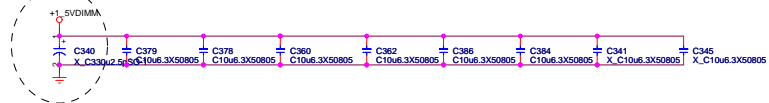
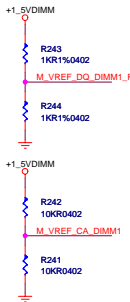
2 x 330u
6 x 1u (per SO-DIMM)

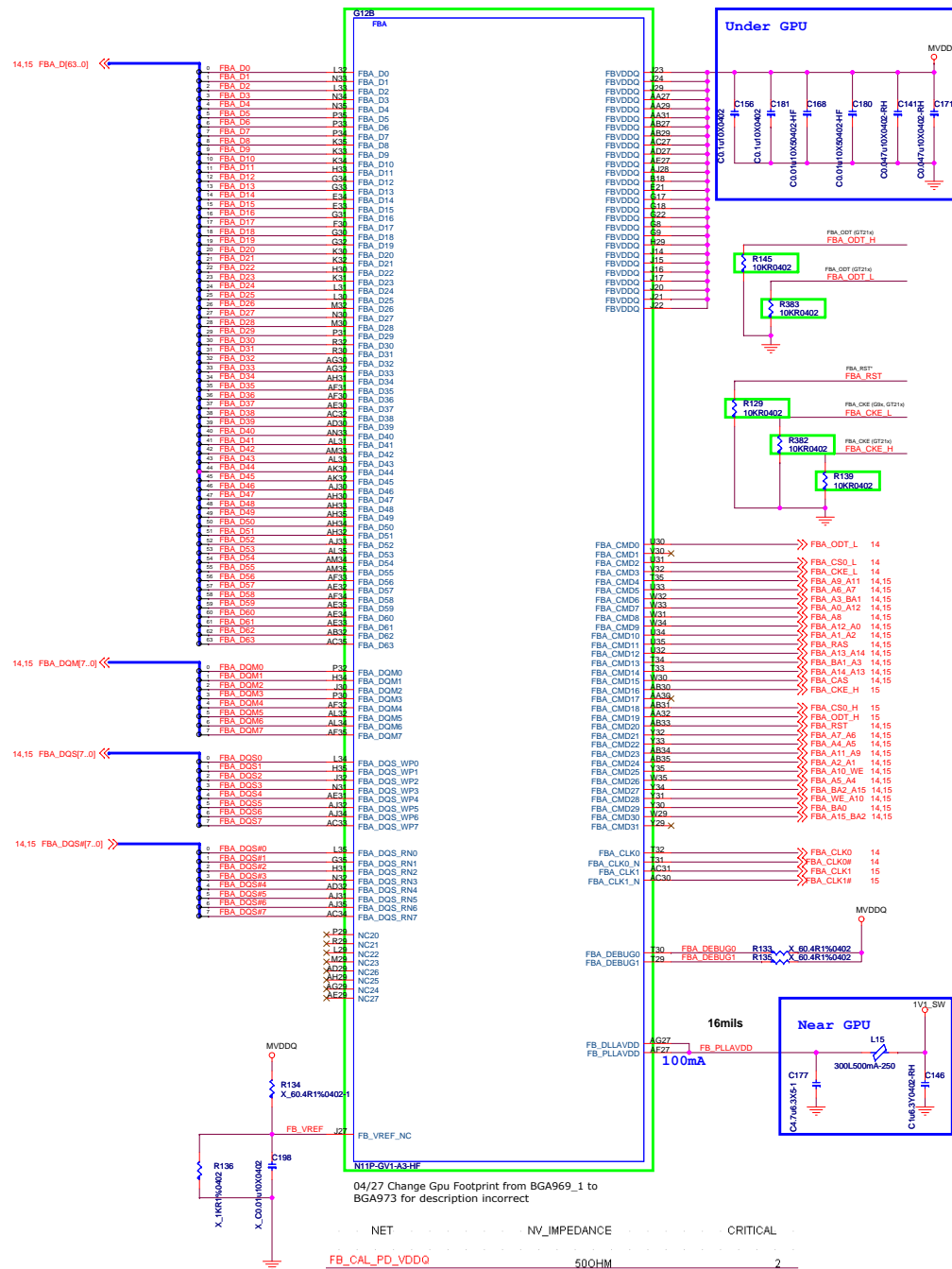
Intel is requesting that customers implement two methods (M1 and M3) to generate and control the DDR3 SO-DIMM Reference voltage for Data/Strobe inputs (V_{REFDDQ}) on Arrandale- and Clarkfield-based platforms. For Arrandale, M1 should be used. For Clarkfield only designs and common motherboard designs (which support both Arrandale and Clarkfield processors), both M1 and M3 methods should be concurrently implemented.

Figure 33. Clarksfield DDR3 SO-DIMM VREF DQ Design Requirements



IDD Specification parameters Definition (IDD values are for full operating range of voltage and Temperature)				
Parameter	Symbol	Max.	Unit	
Operating One bank Active-Precharge current; ICK = ICK(DDO), RRC = IRC(DDO), IRAS = IRASmin(DDO); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	1,200	mA	
Operating One bank Active-Read-Precharge current; ICUT = 0mA, BL = 8, CL = CUIDD, AL = 0; ICK = ICK(DDO), RRC = IRC(DDO), IRAS = IRASmin(DDO), RRD = RRD(DDO); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDCW	IDD1	1,360	mA	
Precharge power-down current; All banks open; ICK = ICK(DDO); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	800	mA	
Precharge quiescent standby current; All banks idle; ICK = ICK(DDO); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDDQ0	960	mA	
Precharge standby current; All banks idle; ICK = ICK(DDO); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	960	mA	
Active power - down current; All banks open; ICK = ICK(DDO); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	800	mA	
Active standby current; All banks open; ICK = ICK(DDO), IRAS = IRASmin(DDO), RRP = RRP(DDO); CKE is HIGH, /CS is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	1,000	mA	
Operating burst read current; All banks open; Continuous burst reads; ICUT = 0mA, BL = 8, CL = CUIDD, AL = 0; ICK = ICK(DDO), IRAS = IRASmin(DDO), RRP = RRP(DDO); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDCW	IDD4R	2,120	mA	
Operating burst write current; All banks open; Continuous burst writes; BL = 8, CL = CUIDD, AL = 0; ICK = ICK(DDO), IRAS = IRASmin(DDO), RRP = RRP(DDO); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD4W	2,320	mA	
Burst refresh current; All banks open; Refresh command at every RRD(DDO) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD6	2,240	mA	
Self refresh current; CK and CKE at DV; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD8	160	mA	
Operating bank interleaved read current; All banks interleaving reads; ICUT = 0mA, BL = 8, CL = CL(DDO), AL = 0; ICK = ICK(DDO), ICK1(DDO), CK1 = CK(DDO), RRC = RRC(DDO), RRD = RRD(DDO), RRD1 = RRD1(DDO); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDCW	IDD7	3,400	mA	





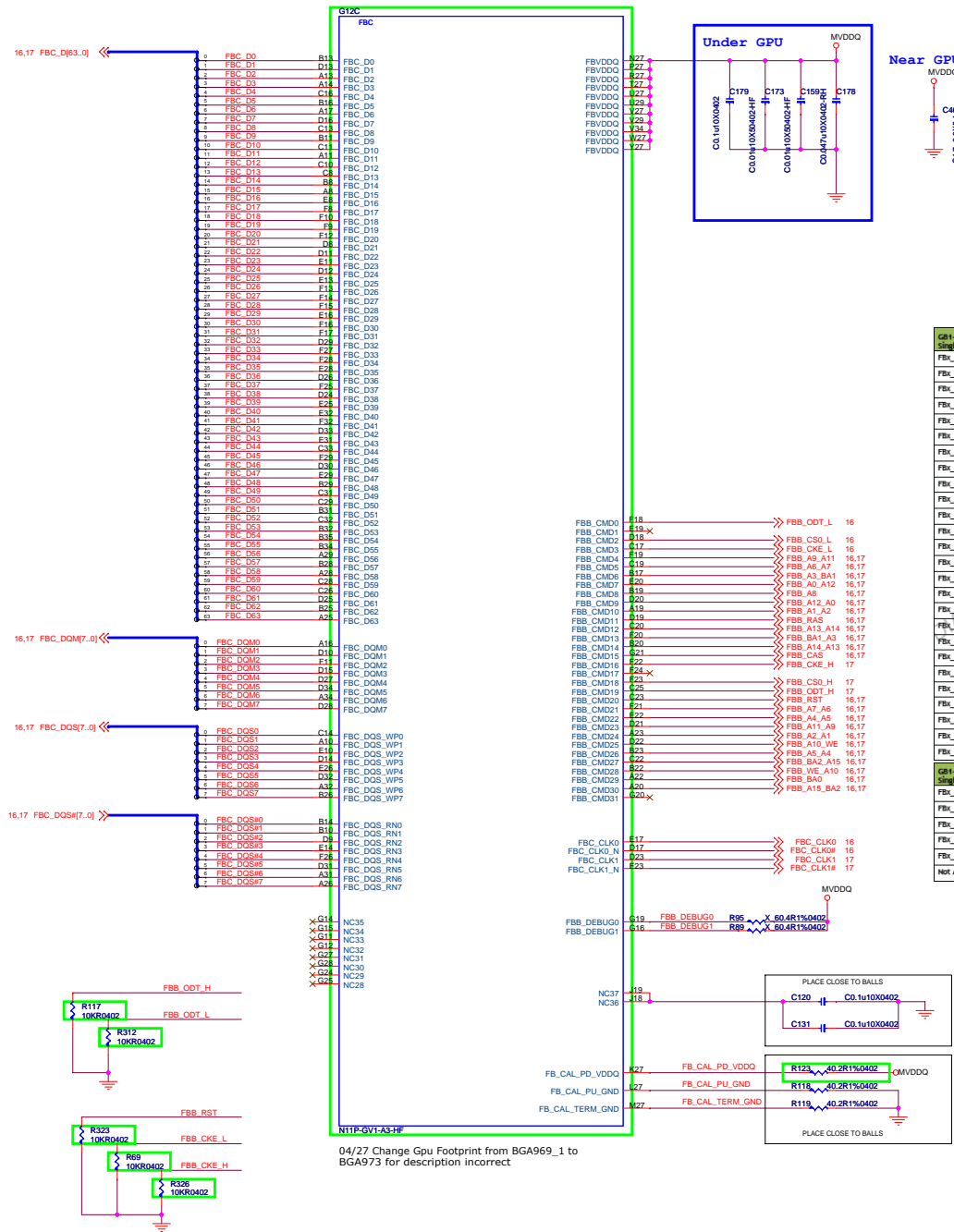
Near GPU



GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
Fbix_CMD0	Fbix_CMD3	CKE	
Fbix_CMD1	Fbix_CMD8	A8	A8
Fbix_CMD2	Fbix_CMD2	CS0*	
Fbix_CMD3	Fbix_CMD21	A7	A6
Fbix_CMD4	Fbix_CMD24	A2	A1
Fbix_CMD5	Fbix_CMD23	A11	A9
Fbix_CMD6	Fbix_CMD26	A5	A4
Fbix_CMD7	Fbix_CMD7	A0	A15
Fbix_CMD8	Fbix_CMD15	CAS*	CAS*
Fbix_CMD9	Fbix_CMD13	BA1	A3
Fbix_CMD10	Fbix_CMD4	A9	A11
Fbix_CMD11	Fbix_CMD18	C50*	
Fbix_CMD12	Fbix_CMD29	BA0	BA0
Fbix_CMD13	Fbix_CMD27	BA2	A15
Fbix_CMD14	Fbix_CMD6	A3	BA1
Fbix_CMD15	Fbix_CMD17		CS1*
Fbix_CMD16	Fbix_CMD19		ODT
Fbix_CMD17	Fbix_CMD22	A4	A5
Fbix_CMD18	Fbix_CMD12	A13	A14
Fbix_CMD19	Fbix_CMD28	WE*	A10
Fbix_CMD20	Fbix_CMD10	A1	A2
Fbix_CMD21	Fbix_CMD25	A10	WE*
Fbix_CMD22	Fbix_CMD9	A12	A0
Fbix_CMD23	Fbix_CMD1	CS1*	
Fbix_CMD24	Fbix_CMD11	RA5*	RA5*
Fbix_CMD25	Fbix_CMD0	ODT	
GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
Fbix_CMD26	Fbix_CMD5	A6	A7
Fbix_CMD27	Fbix_CMD16	CKE	
Fbix_CMD28	Fbix_CMD20	RST	RST
Fbix_CMD29	Fbix_CMD14	A14	A13
Fbix_CMD30	Fbix_CMD30	A15	BA2
Not Available	Fbix_CMD31		

04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

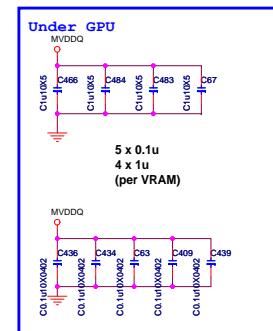
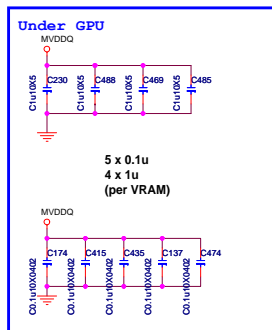
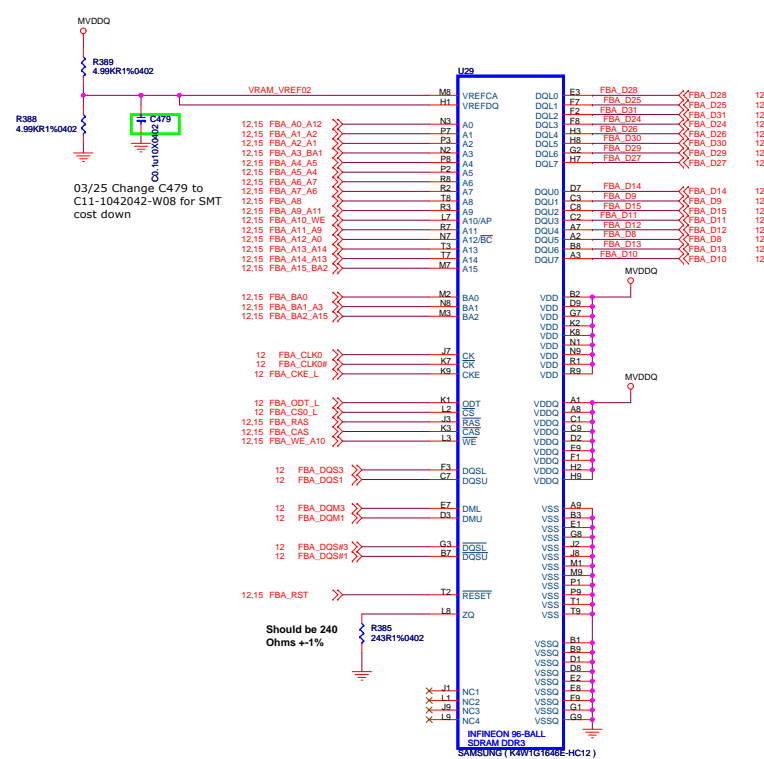
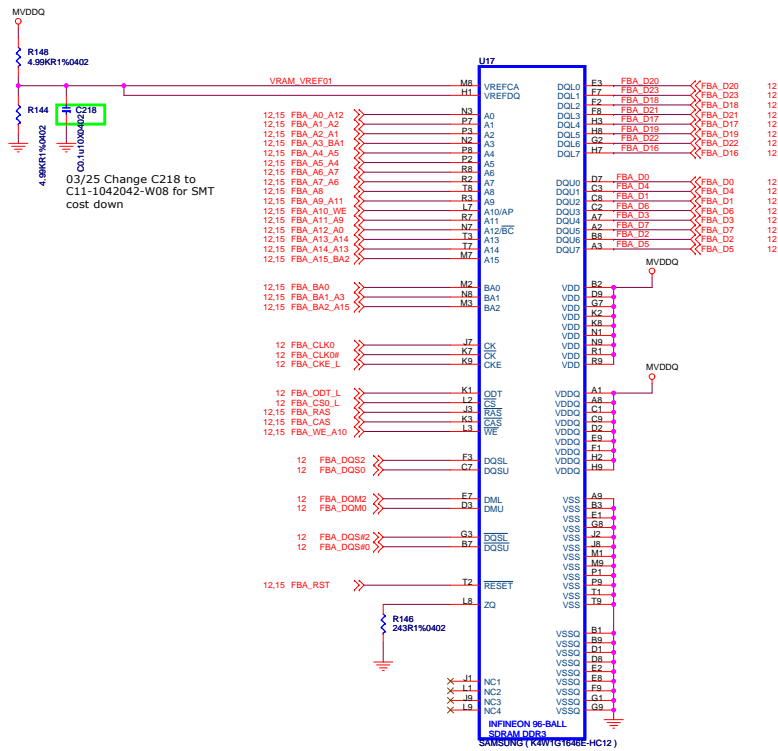
NET	NV_IMPEDANCE	CRITICAL
FB_CAL_PD_VDDQ	50OHM	2
FB_CAL_PU_GND	50OHM	2
FB_CAL_TERM_GND	50OHM	2



GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FbX_CMD0	FbX_CMD3	CKE	
FbX_CMD1	FbX_CMD8	A8	A8
FbX_CMD2	FbX_CMD2	CS0*	
FbX_CMD3	FbX_CMD21	A7	A6
FbX_CMD4	FbX_CMD24	A2	A1
FbX_CMD5	FbX_CMD23	A11	A9
FbX_CMD6	FbX_CMD26	A5	A4
FbX_CMD7	FbX_CMD7	A0	A15
FbX_CMD8	FbX_CMD15	CAS*	CAS*
FbX_CMD9	FbX_CMD13	BA1	A3
FbX_CMD10	FbX_CMD4	A9	A11
FbX_CMD11	FbX_CMD18	CS0*	
FbX_CMD12	FbX_CMD29	BA0	BA0
FbX_CMD13	FbX_CMD27	BA2	A15
FbX_CMD14	FbX_CMD6	A3	BA1
FbX_CMD15	FbX_CMD17		CS1*
FbX_CMD16	FbX_CMD19		ODT
FbX_CMD17	FbX_CMD22	A4	A5
FbX_CMD18	FbX_CMD12	A13	A14
FbX_CMD19	FbX_CMD28	WE*	A10
FbX_CMD20	FbX_CMD10	A1	A2
FbX_CMD21	FbX_CMD25	A10	WE*
FbX_CMD22	FbX_CMD9	A12	A0
FbX_CMD23	FbX_CMD1	CS1*	
FbX_CMD24	FbX_CMD11	RA5*	RA5*
FbX_CMD25	FbX_CMD0	ODT	
GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM function for DQ Bits 0-31	DRAM function for DQ Bits 32-63
FbX_CMD26	FbX_CMD5	A6	A7
FbX_CMD27	FbX_CMD16	CKE	
FbX_CMD28	FbX_CMD20	RST	RST
FbX_CMD29	FbX_CMD14	A14	A13
FbX_CMD30	FbX_CMD30	A15	BA2
Not Available	FbX_CMD31		

NET	NV_IMPEDANCE	CRITICAL
FB_CAL_PD_VDDQ	50OHM	2
FB_CAL_PU_GND	50OHM	2
FB_CAL_TERM_GND	50OHM	2

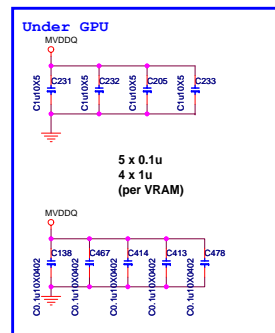
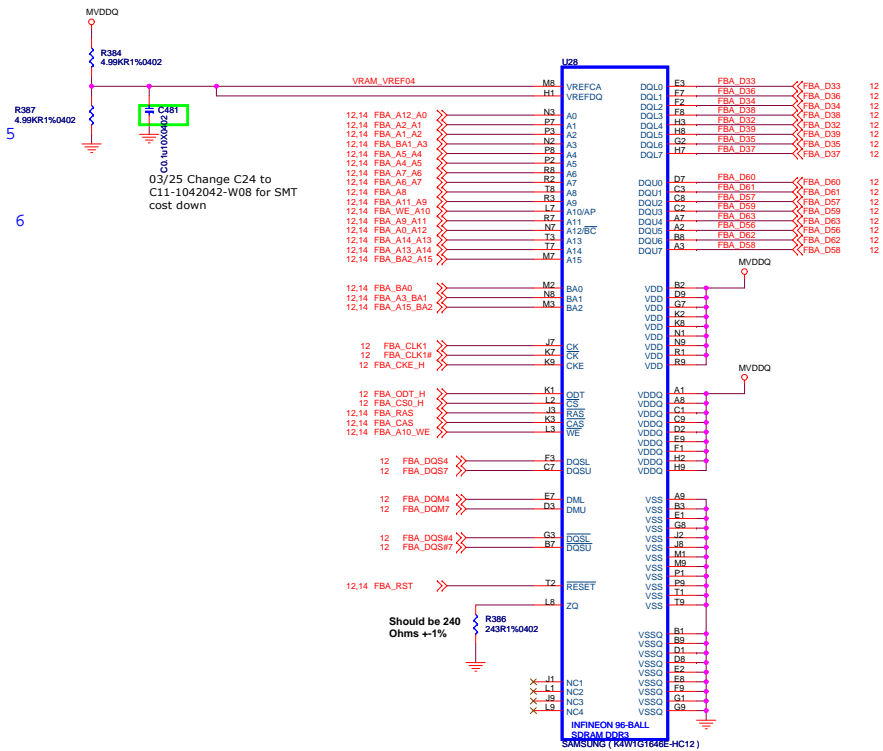
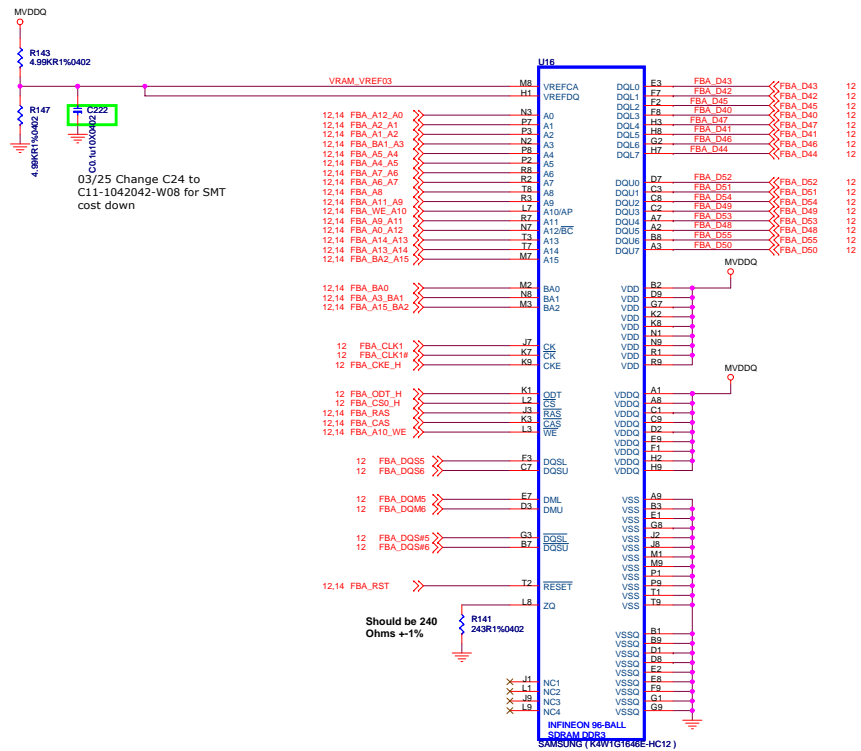
03/19 Change to 40.2R 1% for N11P-GV1 Spec.



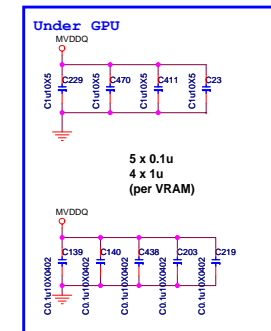
11.0 1Gb gDDR3 SDRAM E-die IDD Spec Table
[Table 44] IDD Specification for 1Gb gDDR3 E-die

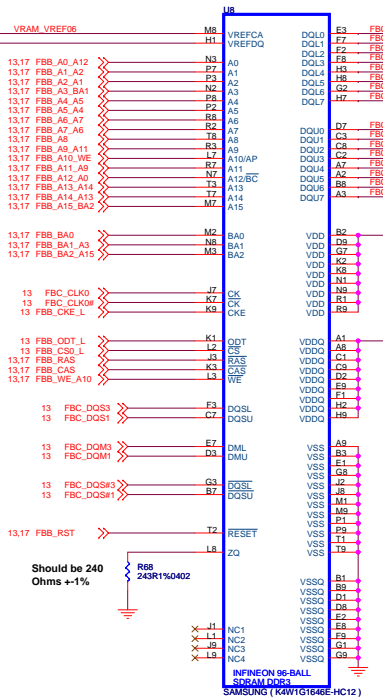
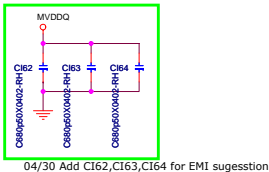
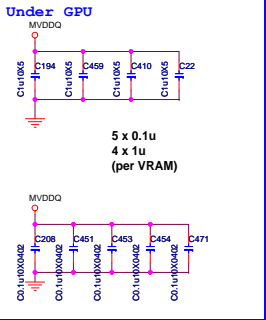
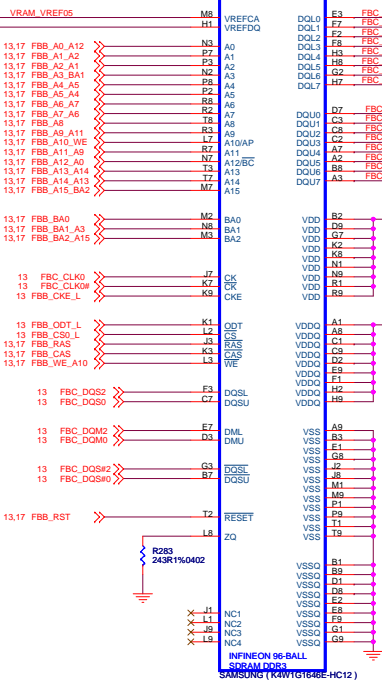
Symbol	64Mx16 (K4W1G1646E)					Unit
	gDDR3-1066 7-7-7	gDDR3-1333 9-9-9	gDDR3-1600 11-11-11	gDDR3-1800 12-12-12	gDDR3-2000 13-13-13	
IDD0	65	70	80	TBD	TBD	mA
IDD1	85	90	105	TBD	TBD	mA
IDD2P-F	25	25	25	TBD	TBD	mA
IDD2P-S	10	10	10	TBD	TBD	mA
IDD2N	30	35	35	TBD	TBD	mA
IDD2Q	30	35	35	TBD	TBD	mA
IDD3P-F	25	27	30	TBD	TBD	mA
IDD3N	45	50	55	TBD	TBD	mA
IDD4R	130	160	200	TBD	TBD	mA
IDD4W	130	155	195	TBD	TBD	mA
IDD5	150	160	160	TBD	TBD	mA
IDD6	10	10	10	TBD	TBD	mA
IDD7	200	240	290	TBD	TBD	mA

NET	MIN_LINE_WIDTH	VOLTAGE
FBA_CLK0_TERM		1.05V
FBA_VREF_DQ0	16MIL	0.9V
FBA_VREF_CA0	16MIL	0.9V
FBA_ZQ0	12MIL	0.9V
FBA_ZQ1	12MIL	0.9V

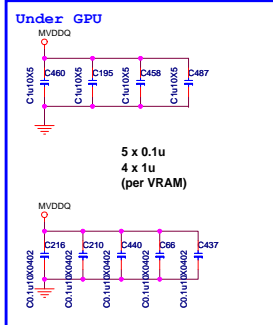


NET	MIN_LINE_WIDTH	VOLTAGE
FBA_CLK0_TERM		1.05V
FBA_VREF_DQ0	16MIL	0.9V
FBA_VREF_CA0	16MIL	0.9V
FBA_ZQ0	12MIL	0.9V
FBA_ZQ1	12MIL	0.9V





NET	MIN_LINE_WIDTH	VOLTAGE
FBC_CU6_TERM		1.05V
FBC_VREF_DQ0	16MIL	0.9V
FBC_VREF_CA0	16MIL	0.9V
FBC_ZQ0	12MIL	0.9V
FBC_ZQ1	12MIL	0.9V



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

04/27 Change Gpu Footprint from BGA969
BGA973 for description incorrect

03/24 Change C65.C68.C80.C443.R76 to NC

04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

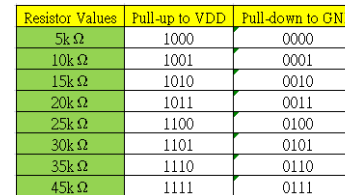
04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

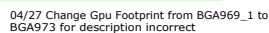
Values	Pull-up to VDD	Pull-down to GND
--------	----------------	------------------

Resistor Values	Full-up to VDD	Full-down to GND
5k Ω	1000	0000
10k Ω	1001	0001
15k Ω	1010	0010
20k Ω	1011	0011
25k Ω	1100	0100
30k Ω	1101	0101
35k Ω	1110	0110
45k Ω	1111	0111

Resistor Values	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]



Resistor Values	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]



Ball Name	Availability	GB1-N11x Normal Function	I/O	Active	Function Description
GPIO0	GB1-64/128	General Purpose	N/A	N/A	
GPIO1	GB1-64/128	HPD-C	I		Hot plug detect for IFP link C
GPIO2	GB1-64/128	LCD0_BL_PWM	O	High	Panel backlight brightness(FWM capable)
GPIO3	GB1-64/128	LCD0_VDD	O	High	panel power enable
GPIO4	GB1-64/128	LCD0_BL_EN	O	High	Panel backlight On/Off(FWM capable)
GPIO5	GB1-64/128	GPU_VID0	O		GPU VID0
GPIO6	GB1-64/128	GPU_VID1	O		GPU VID1
GPIO7	GB1-64/128	GPU_VID2	O		GPU VID2
GPIO8	GB1-64/128	OVERT	I/O	Low	Thermal Catastrophic Overtemp
GPIO9	GB1-64/128	ALERT	I/O	Low	Thermal Alert
GPIO10	GB1-64/128	MEM_VREF	O		Memory VREF switch
GPIO11	GB1-64/128	SLI_SYNC	I/O	Low	SLI raster sync
GPIO12	GB1-64/128	PWR_LEVEL	I		AC power detect input
GPIO13	GB1-64/128	MEM_VID	O		MEM_VID or Power supply control
GPIO14	GB1-64/128	PWR_CTRL1	O		Power supply control
GPIO15	GB1-64/128	HPD-E	I		Hot plug detect for IFP Link E
GPIO16	GB1-64/128	FAN_PWM	O		Programmable Fan Control
GPIO17	GB1-64/128	Reserved	I		
GPIO18	GB1-64/128	Reserved	I		
GPIO19	GB1-64/128	HPD-D	I		Hot plug detect for IFP Link D
GPIO20	GB1-64/128	Reserved	I		
GPIO21	GB1-64/128	HPD-F	I		Hot plug detect for IFP Link F
GPIO22	GB1-64/128	SWAPRDY			SLI swap ready signal
GPIO23	GB1-64/128	STEREO	I/O		

DA-04661-001_v04
DA-04882-001

Products	GPU (W)	Mem (W)	NVCLK/MCLK (MHz)
N11P-GE1 1024MB DDR3	22.98	5.07	575/790
N11P-LP1 1024MB DDR3	14.81	4.78	475/700
N11P-GS1 1024MB DDR3	22.85	4.97	450/790

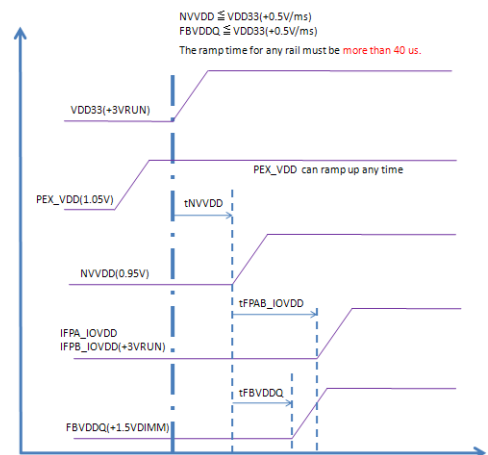
Products	NVVD
N11P-GE1 1024MB DDR3	0.95V
N11P-LP1 1024MB DDR3	0.85V
N11P-GS1 1024MB DDR3	0.9V

Products	FBVDD 1.5V	FBVDDQ GPU+Mem 1.5V
N11P-GE1 1024MB DDR3	1.84A	2.76W
N11P-LP1 1024MB DDR3	1.69A	2.54W
N11P-GS1 1024MB DDR3	1.52A	2.28W

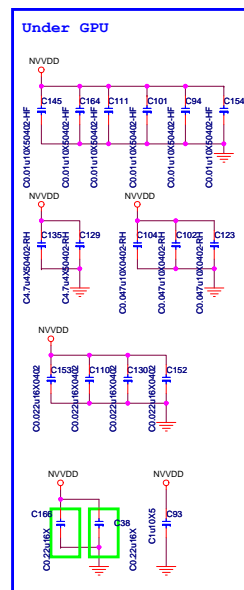
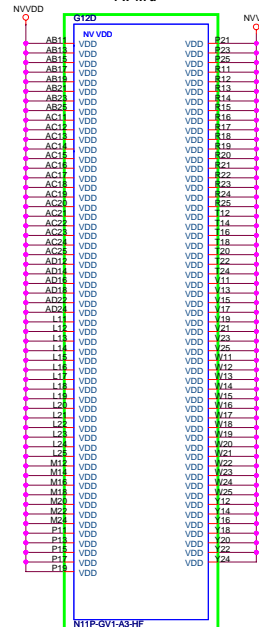
Products	PCI Express 1.05V	I/O PLLVDD 1.05V
N11P-GE1 1024MB DDR3	599.27mA	0.63W
N11P-LP1 1024MB DDR3	581.74mA	0.61W
N11P-GS1 1024MB DDR3	578mA	0.61W

Products	I/O PLLVDD 1.8V
N11P-GE1 1024MB DDR3	88.5mA
N11P-LP1 1024MB DDR3	88.5mA
N11P-GS1 1024MB DDR3	87mA

Products	Other 3.3V
N11P-GE1 1024MB DDR3	39.97mA
N11P-LP1 1024MB DDR3	39.97mA
N11P-GS1 1024MB DDR3	39mA



2 x 4700p
6 x 0.01u
4 x 0.022u
3 x 0.047u
2 x 0.22u
1 x 1u
1 x 4.7u



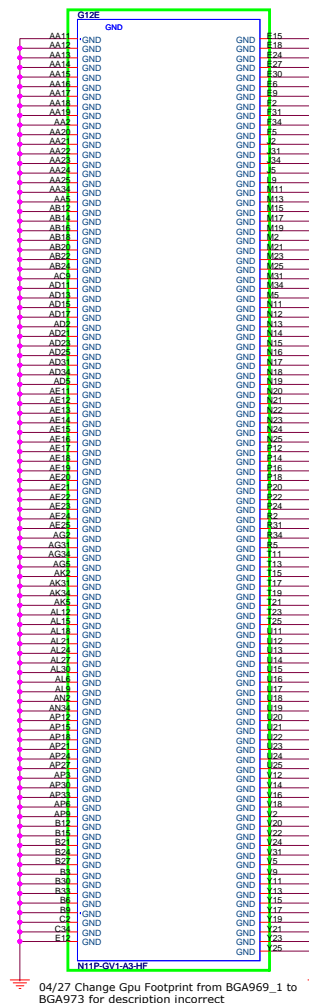
Change C38.C166 from C11-2242033-S02 to C11-2242013-W08 for SMT cost down

Near GPU



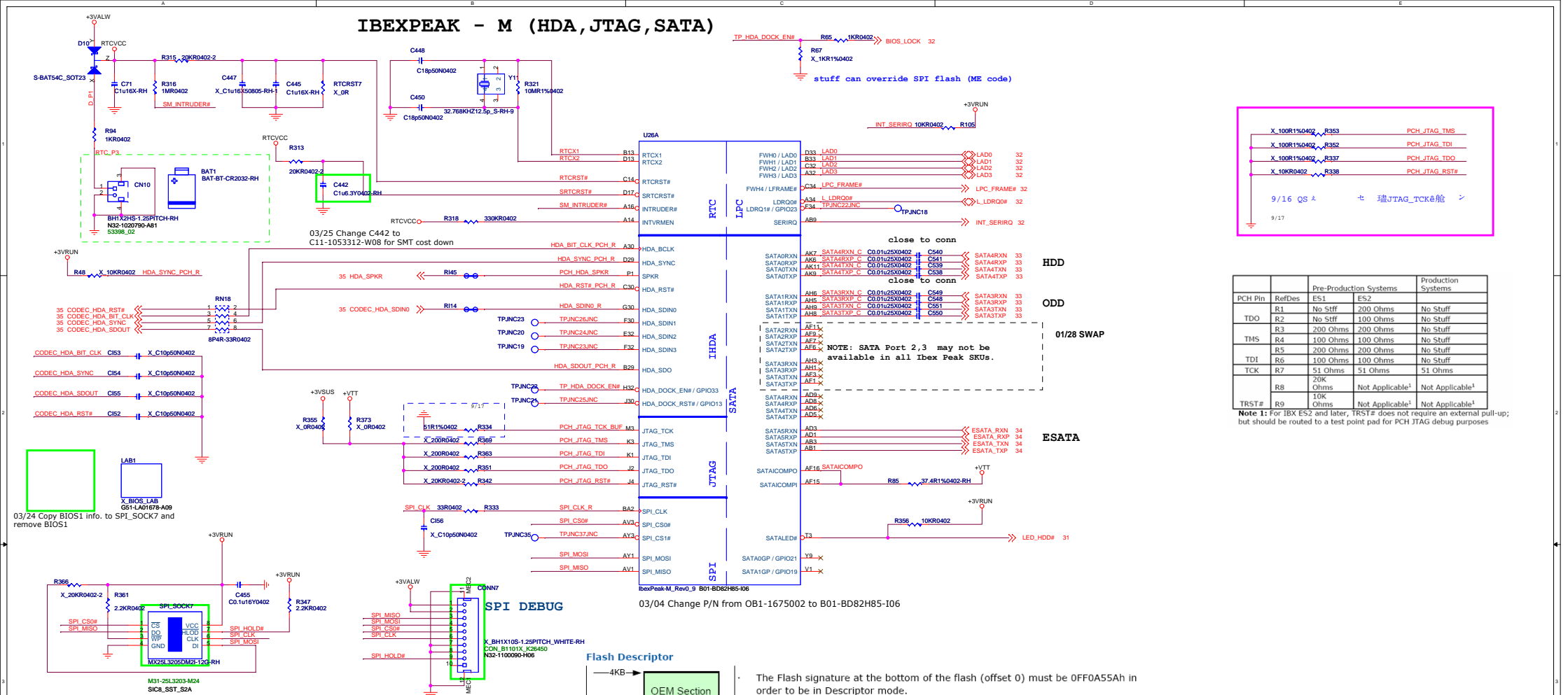
04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

Products	GPU (4)	Mem (1.5)	NVCLK /MCLK	NVVDD		FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05 V) (6)		I/O and PLLVD (1.8V)		I/O and PLLVD (1.05V)		Other (3.3 V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)
N11P-GV1 (128-bit, 1024 MB, DDR3)	16.01	4.72	450/700	0.85	15.82	13.45	1.66	2.49	2.47	3.71	572	0.60	88.50	0.16	186.77	0.20	39.97
																	0.13



04/27 Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect

IBEXPEAK - M (HDA, JTAG, SATA)



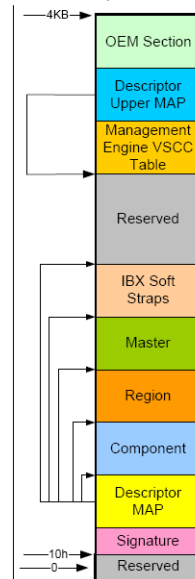
Boot Flow for Ibex Peak

When booting from Global Reset the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 at address 0x0. The descriptor fetch is triggered whichever comes first, **the assertion of MEPWROK or deassertion of LAN_RST#**. If the signature is present and valid, then the PCH controller will boot in Descriptor mode. It will load up the descriptor into corresponding registers in the PCH. If the signature is NOT present the PCH will boot in non descriptor mode where integrated LAN and all Intel Management Firmware will be disabled. Whether there is a valid descriptor or not, the PCH will look to the GNT0# and SPL_CS1#1 (Boot BIOS Destination straps) to determine if BIOS is to be booted from Firmware hub or SPI flash.

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Ix86 Peak based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers. The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.


Flash Descriptor



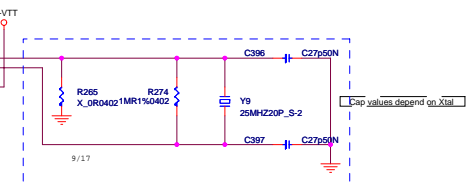
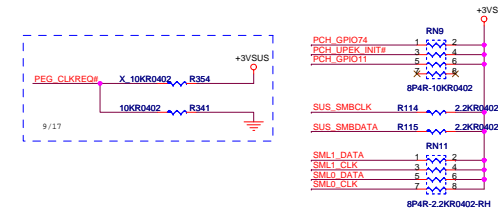
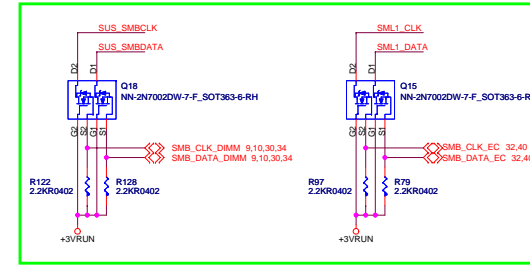
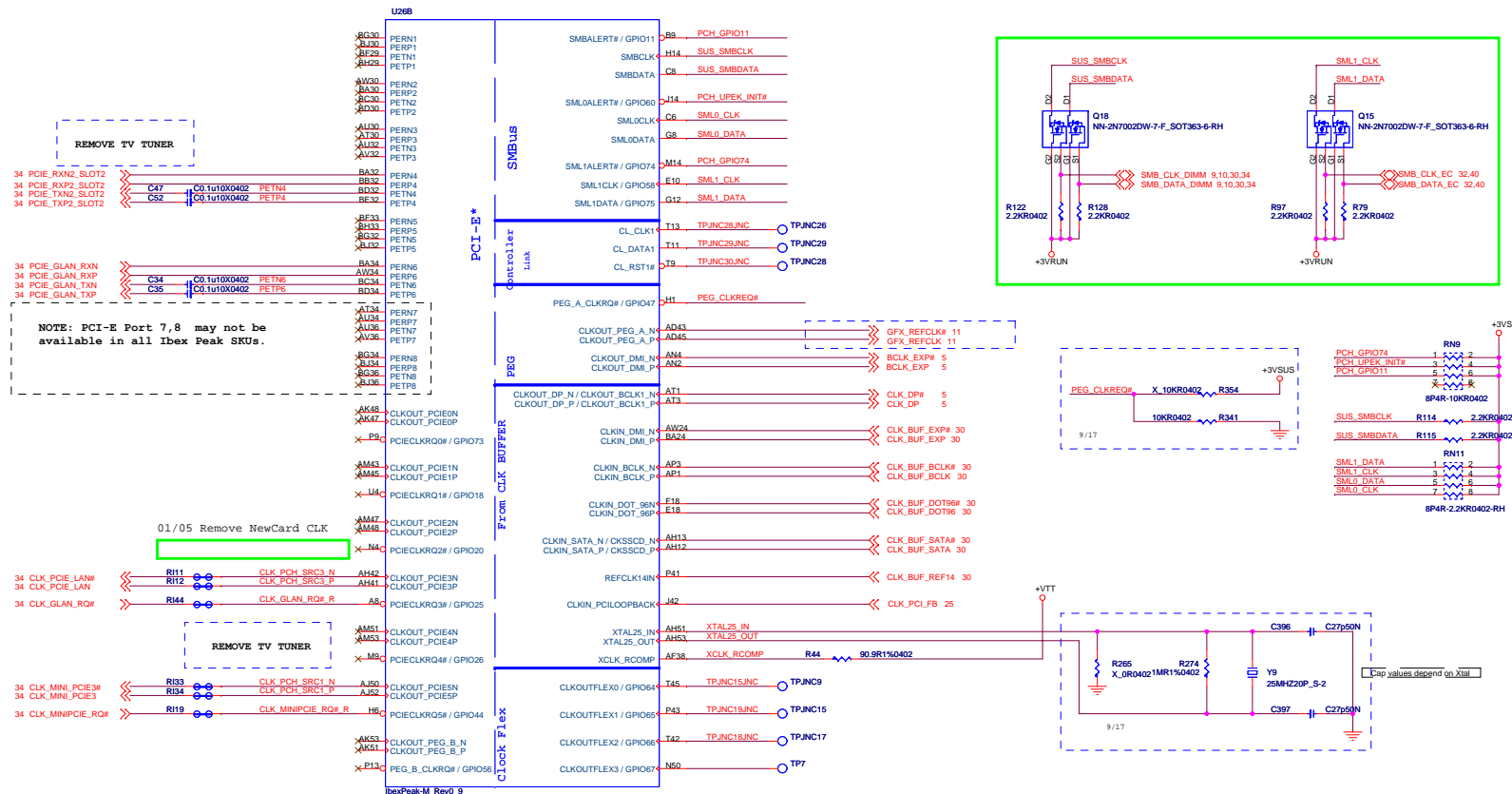
- The Flash signature at the bottom of the flash (offset 0) must be OFF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, ME and GbE regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel® ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image. This table is **NOT used by Intel® ME** Ignition FW only. BIOS and GbE write and erase capabilities depend on **LVSCC and UVSCC** registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

Region Access Control Table

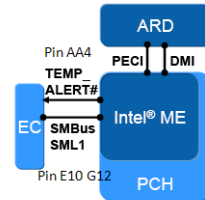
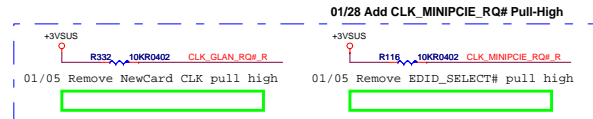
Master Read/Write Access			
Region	CPU and BIOS	ME	GbE Controller
Descriptor	N/A	N/A	N/A
BIOS	CPU and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Management Engine	Read / Write	ME can always read from and write to ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

 MICRO-STAR INT'L CO.,LTD.	
Title IBEXPEAK - M (HDA,JTAG,SATA)	
Size Custom	Document Number MS-16G1
Date: Tuesday, May 04, 2010	Sheet 21 of 56 Rev QA

IBEXPEAK - M (PCI-E, SMBUS, CLK)



PCIECLKRQ1# / GPIO18 PCIECLKRQ2# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well



- Turbo Boost control- EC passes parameters through PCH to host software for real-time Turbo Boost control.
- PCH can be programmed to notify EC when a device is outside of limits via TEMP_ALERT# signal- No SW alert in PCH.

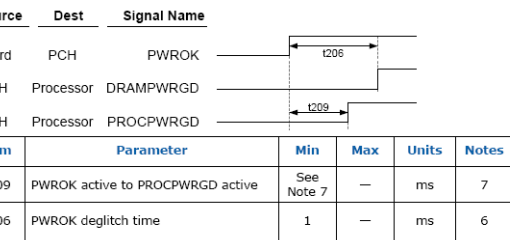
- EC can read from PCH via SMBus:
 - Temperatures
 - CPU, GMCH
 - Sequence number
 - Host status
- EC can write to PCH via SMBus:
 - Disable and enable power sharing
 - CPU and package power clamps
 - Biasing preference
 - Upper and lower temperature limits
 - CPU, MCH
 - TEMP_ALERT# trip points
- PCH can alert EC to out of range temperature conditions
 - TEMP_ALERT# signal assertion

- EC can monitor Intel® ME health by checking "Sequence Number"
 - Increments each time the Intel ME refreshes data
- Indicates optional usage with Turbo Boost

Byte	Data	Format	Units	Range
0	Max. Package Temperature	Unsigned byte	1°C/bit	0-255°C
1	PCH Temperature	Unsigned byte	1°C/bit	0-255°C
3:2	CPU Temperature	10.6 Format	1/64°C/bit	0-256°C
4	MCH Temperature	Unsigned byte	1°C/bit	0-255°C
5	DIMM0 Temperature	Unsigned byte	1°C/bit	0-255°C
6	DIMM1 Temperature	Unsigned byte	1°C/bit	0-255°C
7	DIMM2 Temperature	Unsigned byte	1°C/bit	0-255°C
8	DIMM3 Temperature	Unsigned byte	1°C/bit	0-255°C
9	Sequence Number	Unsigned byte	Count	0-255
13:10	CPU Energy Counter	16 int:16frac	0.125J/bit	N/A
19:14	Host Status	Status register	N/A	N/A

Commands	Format	Units
SMBus Turbo Status (STS)	Register	
CPU Temperature Limits	10.6 Format	1/64°C/bit
MCH Temperature Limits	Unsigned byte	1°C/bit
IBX Temperature Limits	Unsigned byte	1°C/bit
DIMM Temperature Limits	Unsigned byte	1°C/bit
Processor Power Clamp	Unsigned word	0.1W/bit

The Flexible Display Interface (Intel® FDI) is a bus technology that utilizes differential signaling to transport display data from a pixel source Havendale to a sink Ibox Peak. There are two Flexible Display Interface channels- A and B which are independently controlled. Each channel from Havendale include 4 Tx differential pairs comprising the data link, used for transporting pixel and framing data from the display engine. Two single-ended LineSync and FrameSync inputs. Single-ended DISP_INT is used for interrupts from sink (Ibox Peak) to source (Havendale).

[illegible]

6. Ensure PWROK is a solid logic '1' before proceeding with the boot sequence. Note: If PWROK drops after t206 it will be considered a power failure.
7. t209 minimum timing selectable as 1 ms (recommended), 5 ms, 50 ms, or 100 ms using bits 9:8 of PCHSTRP15.

IBEXPEAK - M (LVDS,DDI)

DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

03/26 Change R41 and R39 Footprint from 0R0402 to NC_0402_6 for cost down

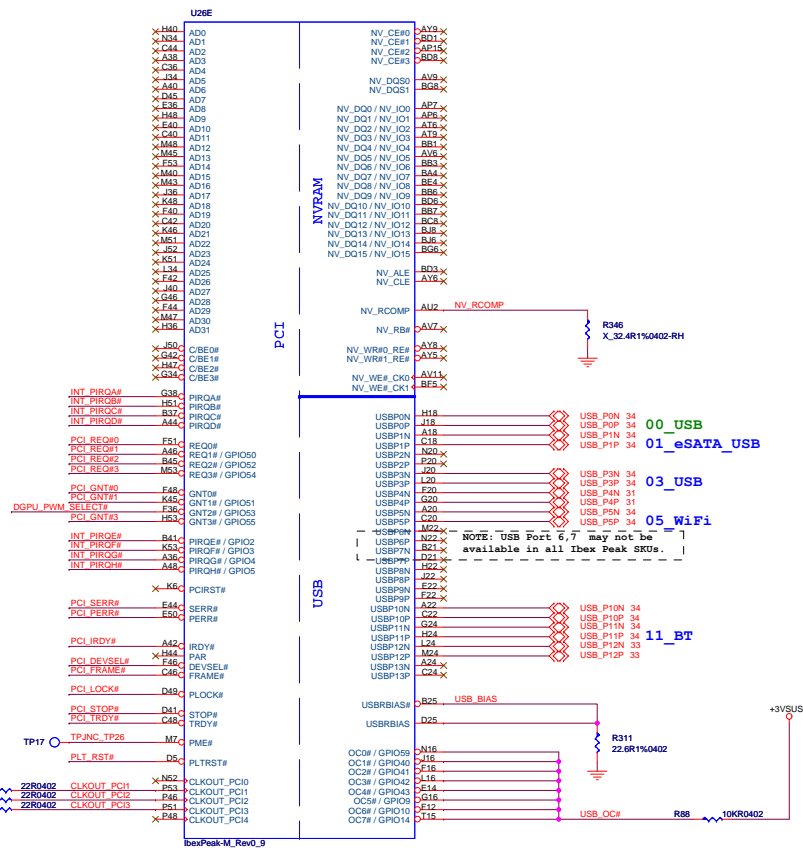
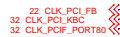
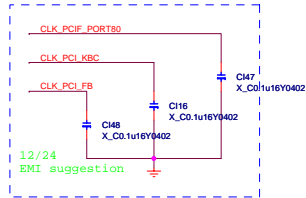
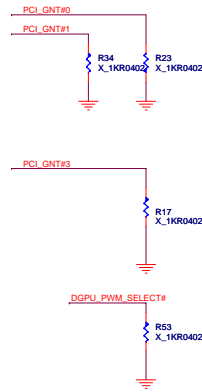
1. MCM only LVD_1BG, LVD_VREFH and LVD_VREFL floating. VCCA_LCD and VCCITX_LVD can be connected to GND.
2. If use LVDS, LVD_1BG connect 2.37k to GND. LVD_VREFH and LVD_VREFL connect to GND. VCCA_LCD and VCCITX_LVD connect to power.

37.5ohm : 7/10/20 , 8/10/20 , 800mils

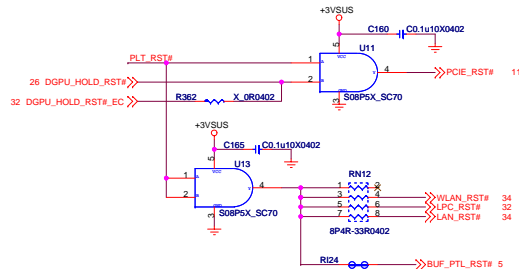
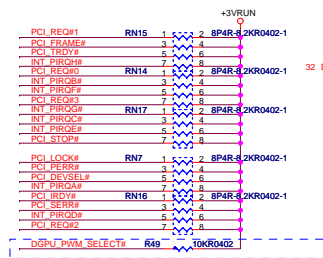
IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

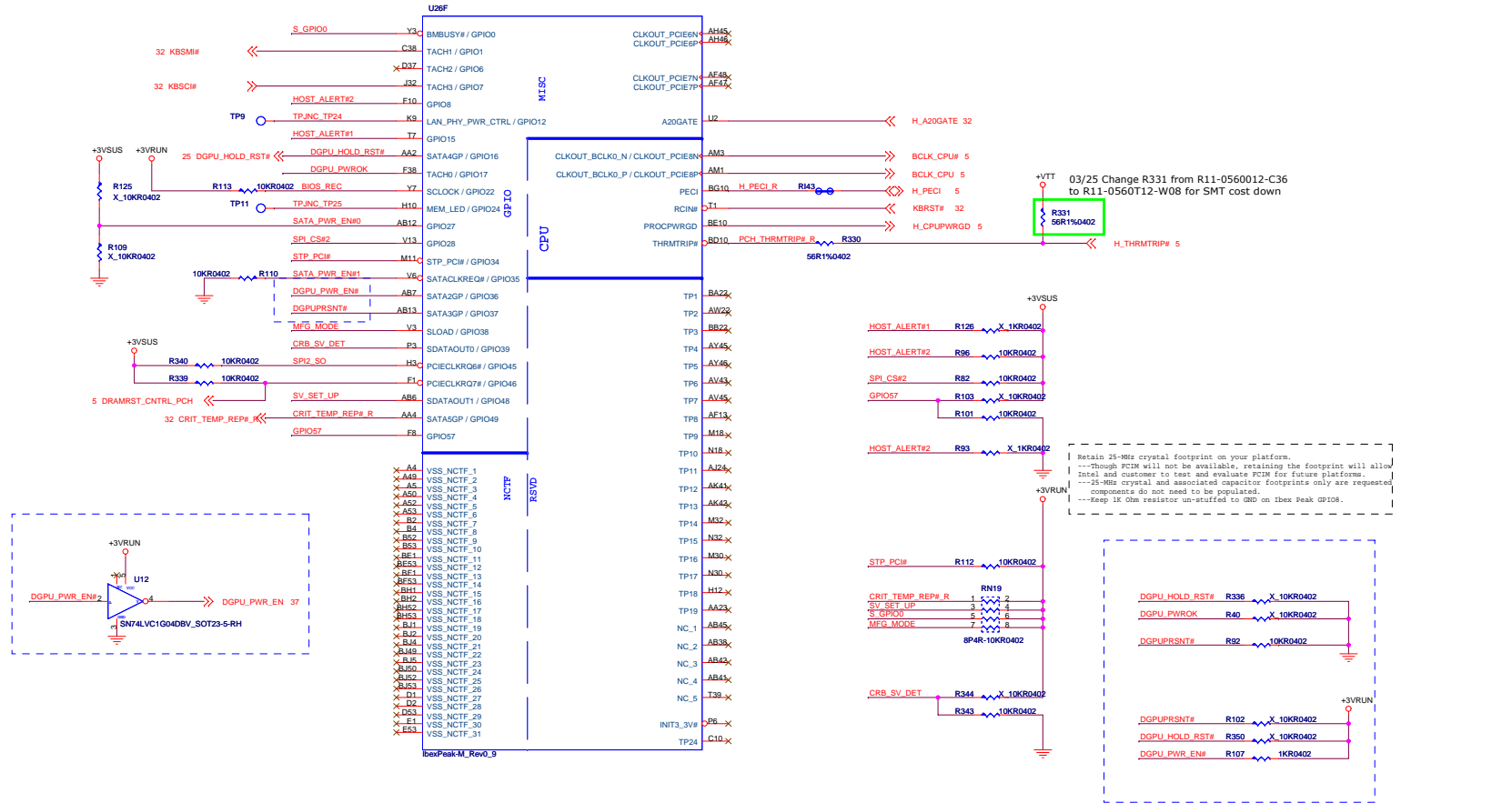
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	LOW = A16 swap override/Top-Block Swap Override enabled High = Default



EHCI 1 : 0~7
EHCI 2 : 8~13



IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



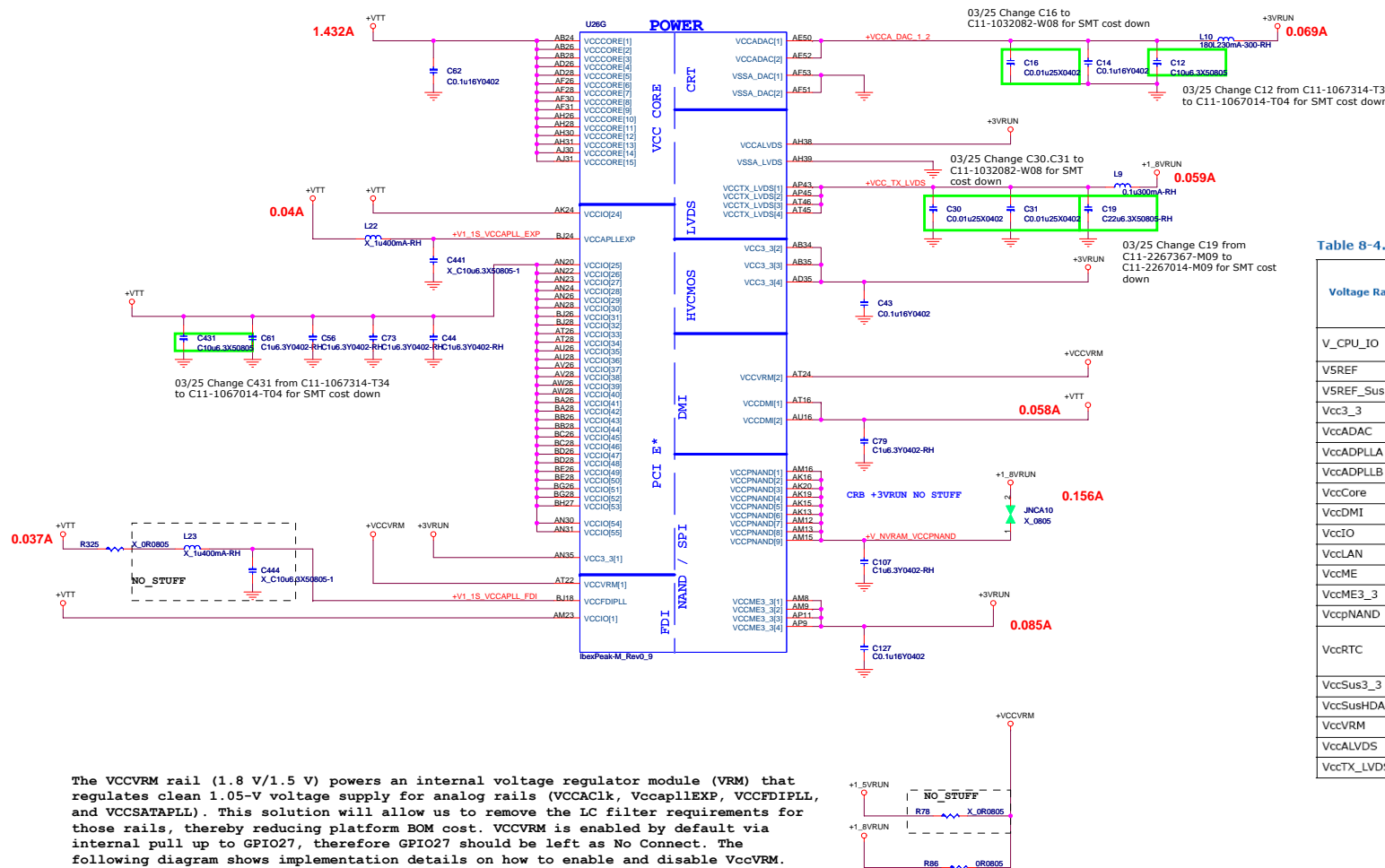
03/25 Change C7 to C11-1043062-W08 for SMT cost down

03/25 Change C431 from C11-1067314-T34 to C11-1067014-T04 for SMT cost down

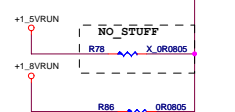
03/25 Change R331 from R11-0560012-C36 to R11-0560T12-W08 for SMT cost down

Retain 35-MHz crystal footprint on your platform.
 ---Though PCM will not be available, retaining the footprint will allow Intel and customer to test and evaluate PCM for future platforms.
 ---25-MHz crystal and associated capacitor footprints only are requested components do not need to be populated.
 ---Keep 1K Ohm resistor un-stuffed to GND on IbeX Peak GPIO8.

IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



Mobile Thermal Design Power

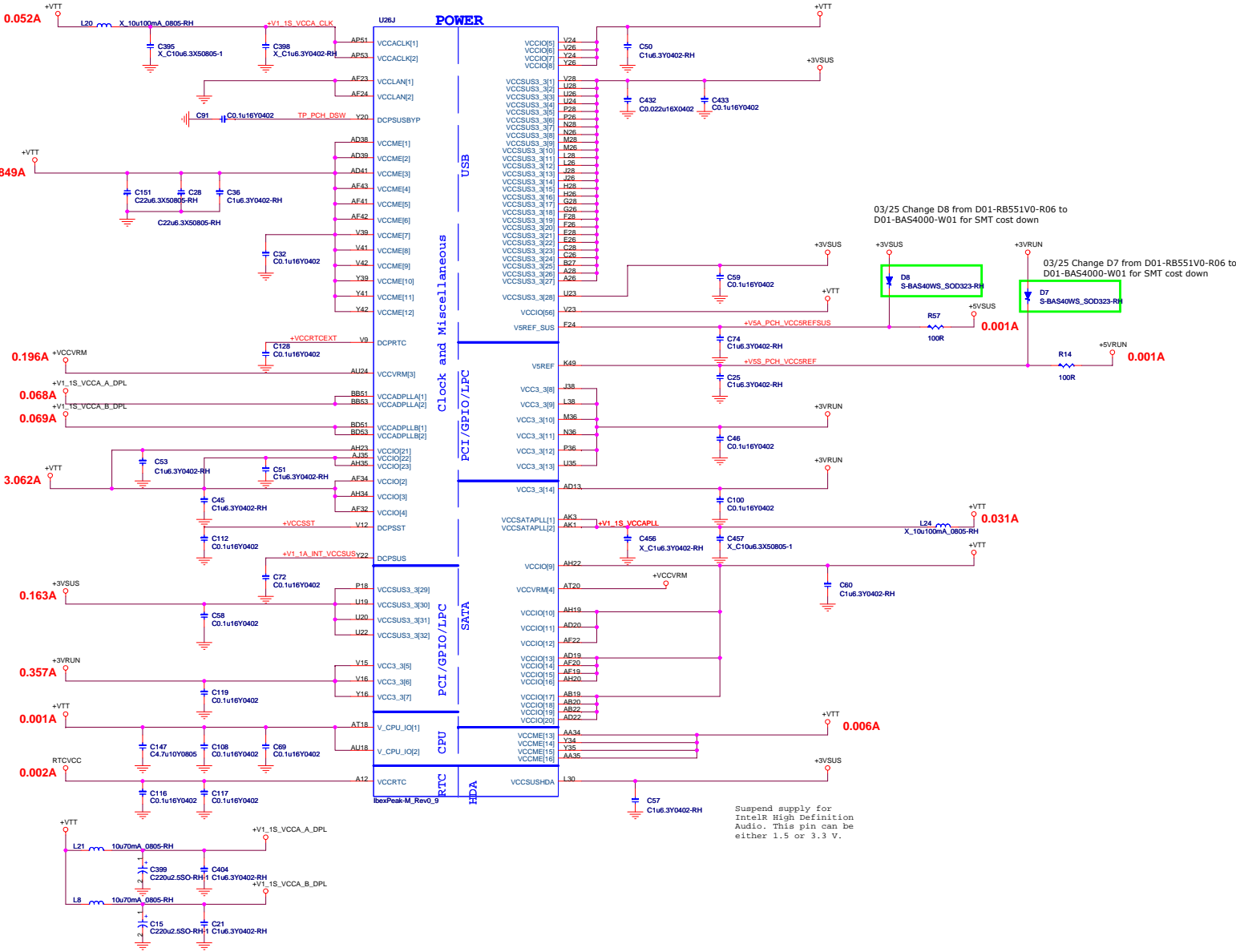
SKU	Thermal Design Power (TDP)	Notes
QM57	3.5 W	1
HM57	3.5 W	1
HM55	3.5 W	1
PM55	3.5 W	1
QS57	3.4 W	1

Table 8-4. Measured I_{CC} (Mobile Only)

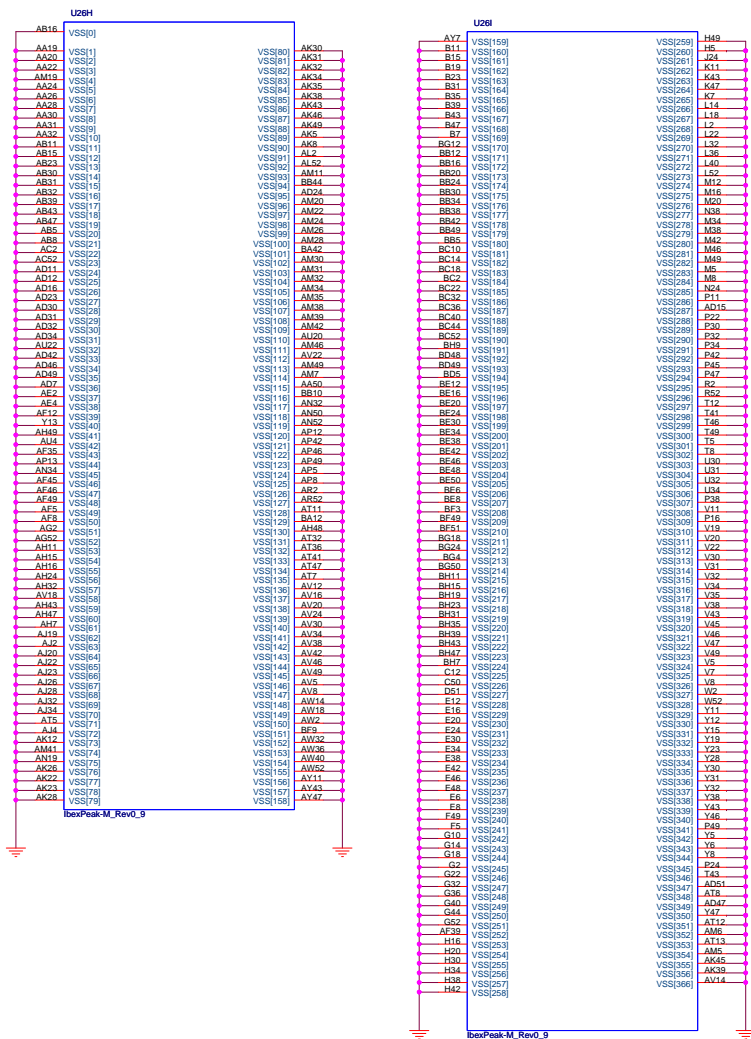
Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
V_CPU_IO	1.1/1.05	.001	.001	.001	.001			—
V5REF	5	.001	.001	.001	.001			—
V5REF_Sus	5	.001	.001	.001	.001	.001		—
Vcc3_3	3.3	.305	.305	.0176	.0176			—
VccADAC	3.3	.075	.0011	.0011	.0011			—
VccADPLL	1.05	.088	.0176	.825	.0044			—
VccADPLL	1.05	.088	.0176	.0044	.0044			—
VccCore	1.05	1.43	1.254	.3685	.2805			—
VccDMI	1.1	.055	.055	.0011	.0011			—
VccIO	1.05	3.23	2.628	.463	.285			—
VccLAN	1.05	.220	.220	.066	.066	.132		—
VccME	1.05	1.2	1.2	.186	.186	.98	.0044	—
VccME3_3	3.3	.031	.031	.0022	.0022	.0154	.0022	—
VccpNAND	1.8	.0055	.0055	.0022	.0022			—
VccRTC	3.3	.0011	.0011	.0011	.0011	.0011	.0011	6 uA See notes 1, 2
VccSus3_3	3.3	.087	.087	.0132	.0132	.133	.0297	—
VccSusHDA	3.3	.0088	.0088	.001	.001	.001	.001	—
VccVRM	1.8/1.5	.156	.114	.113	.045			—
VccALVDS	3.3	.0011	.0011	.0011	.0011			—
VccTX_LVDS	1.8	.066	.0011	.0198	.0011			—

VccLAN may be grounded if Intel LAN is disabled.

IBEXPEAK - M (POWER)



IBEXPEAK - M (GND)



Intel® 5 Series Chipset Mobile SKUs

Feature Set		SKU Name(s)				
		QM57	HM57	PM55	HM55	QSS7
PCI Express* 2.0 Ports		8	8	8	6 ⁵	8
USB* 2.0 Ports		14	14	14	12 ⁴	14
SATA Ports		6	6	6	4 ⁶	6
HDMI/DVI/VGA/SDVO/DisplayPort		Yes	Yes	No	Yes	Yes
LVDS		Yes	Yes	No	Yes	Yes
Graphics Support with PAVP 1.5		Yes	Yes	No	Yes	Yes
FIS Based Port Multiplier Support		Yes	Yes	Yes	No	Yes
Intel® Quiet System Technology		No	No	No	No	No
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	Raid 0/1/5/10 Support	Yes	Yes	Yes	No	Yes
Intel® ME Ignition FW only		No	No	Yes	No	No
Intel® AT		Yes	Yes	No	Yes	Yes
Intel® AMT 6.0		Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Business		Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Consumer		No	Yes	No	No	No
Intel® Remote Wake Technology		No	No	No	No	No

Figure 2-6. Platform Power Block Diagram—S3, M-Off, with WoL, No WoWLAN

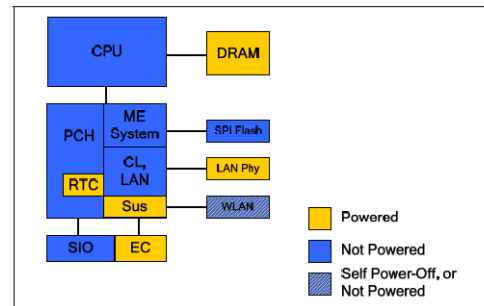


Figure 2-9. Platform Power Block Diagram—S4-S, M-Off, with WoL, No WoWLAN

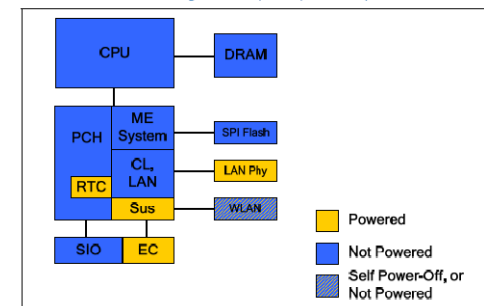
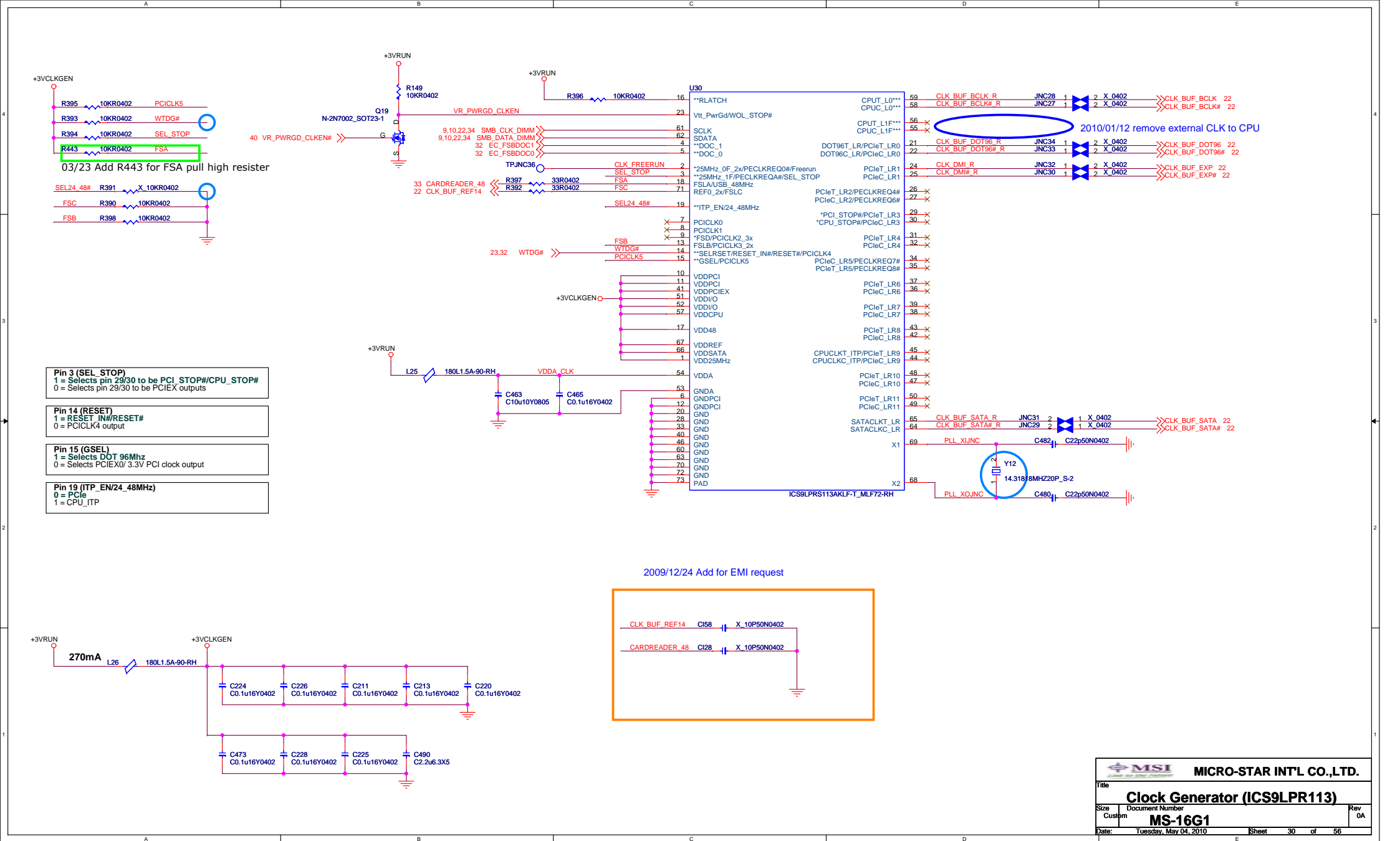
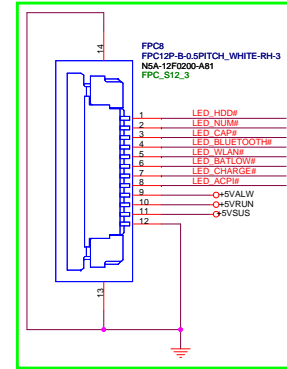
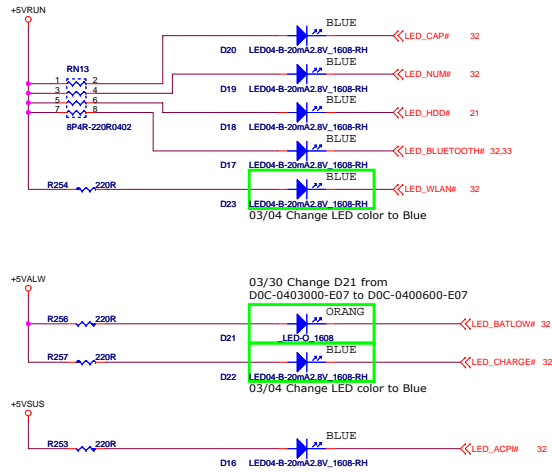


Table 113. Power Delivery Summary for Intel Management Engine SubSystem (Sheet 1 of 2)

What It Powers	Rail	Sx ¹ /M3	Sx/Moff ²	Sx/Moff/WOL ³	Source	Enabled By	Power OK indicator
Platform 5-V Rail	V5.0A	On	On	On	5 V Always (5x)		
DRAM VDD	V1.5U	On in S3	On in S3	On in S3	V1.5U	SLP_S4#	
DRAM VTT	V0.75S or V0.75U	Off ⁴	Off ⁴	Off ⁴	V0.75S or V0.75U	SLP_S3#	
CK505	3.3 CK505	Off ⁵	Off ⁵	Off ⁵	V3.3S	CKPWRGD	
Mobile Intel® 5 Series Chipset	1.05 VCORE	Off ⁵	Off ⁵	Off ⁵	V1.05S		PWROK
WLAN	V3.3A	On	On	On	3.3 V Always		
M3 Support + Intel® 82577 GbE LAN							
Intel® ME Local RAM	V1.05M	On	Off	Off	V1.05M	SLP_M# ⁶	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	On	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	On	Off	Off ⁷	V3.3M	SLP_M# ⁶	MEPWROK
Integrated LAN controller	VCCLAN	On	Off	Off	V1.05M	SLP_M# ⁶	
No M3 Support + Intel® 82577 GbE LAN							
Intel ME Local RAM	V1.05M	Off	Off	Off	V1.05M	SLP_M# ⁶	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	Off	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off ⁷	V3.3M	SLP_M# ⁶	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	Grounded		
No M3 Support + No Intel® 82577 GbE LAN							
Intel ME Local RAM	V1.05M/1.1M	Off	Off	Off	V1.05M	SLP_M# ⁶	MEPWROK
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off ⁷	V3.3M	SLP_M# ⁶	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	Grounded		

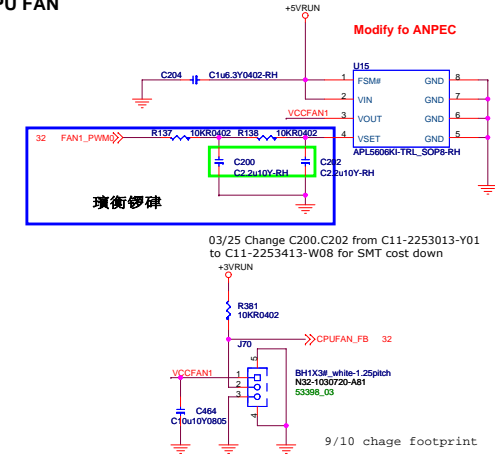


LED

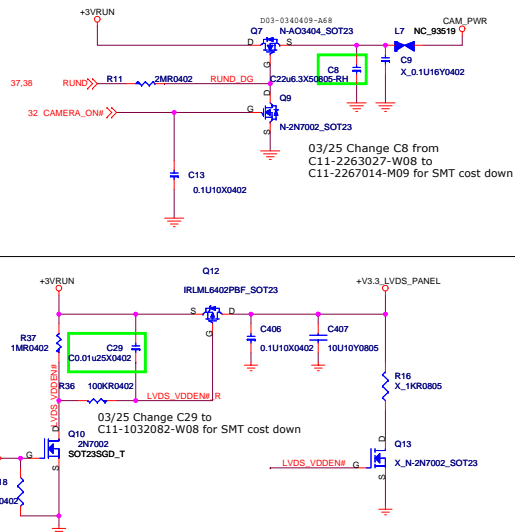


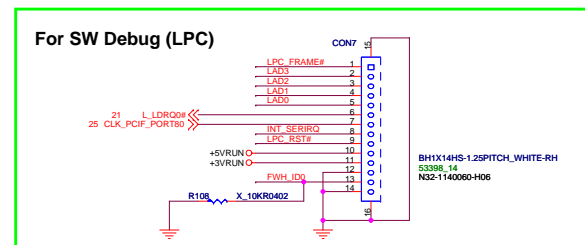
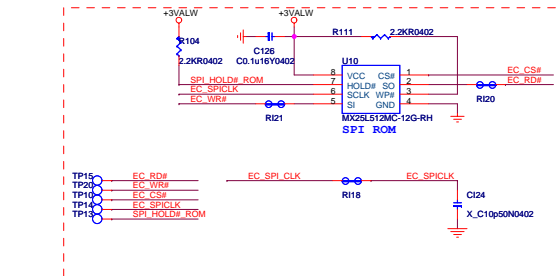
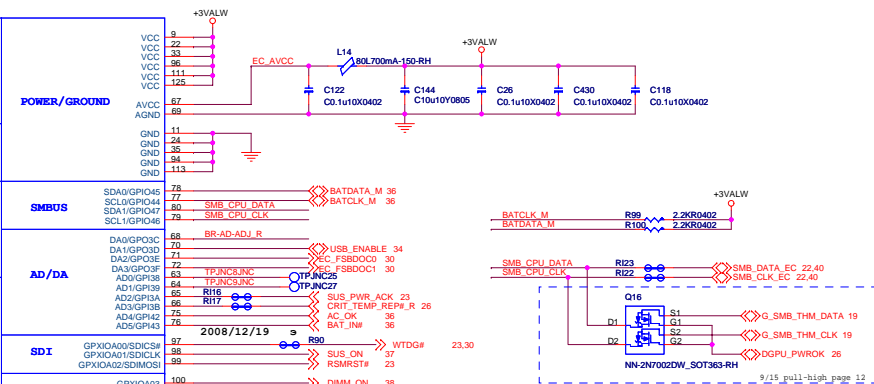
03/25 Move ODM LED Function to MB

CPU FAN

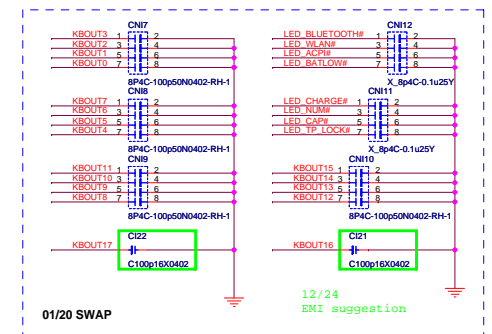
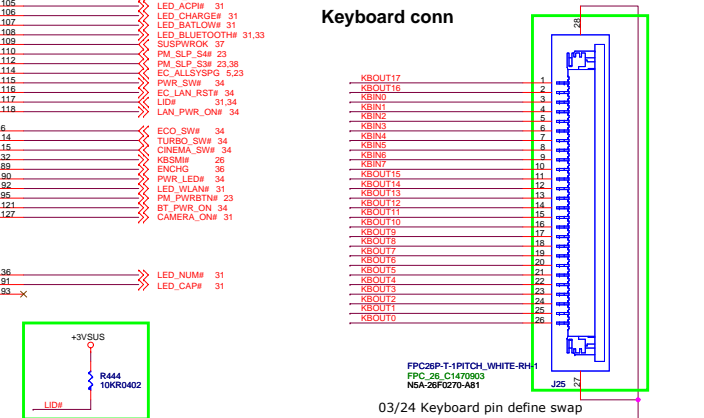
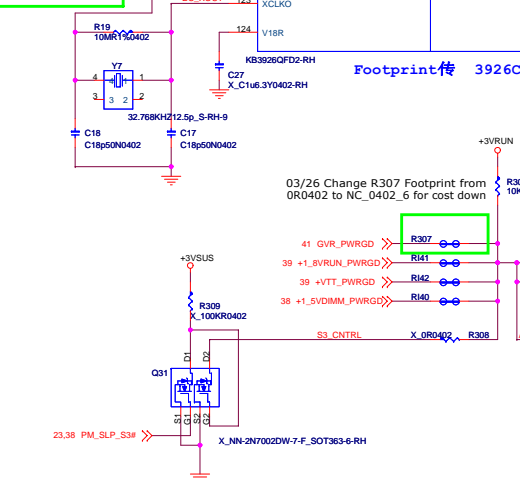
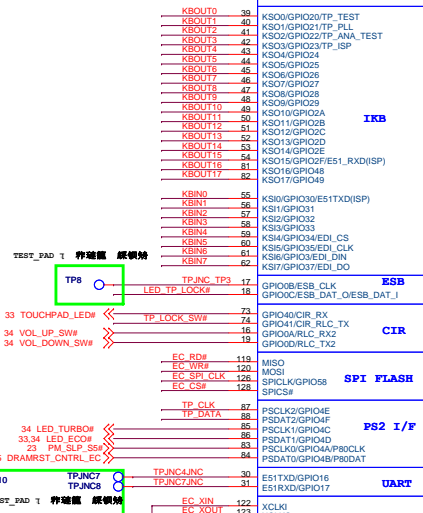
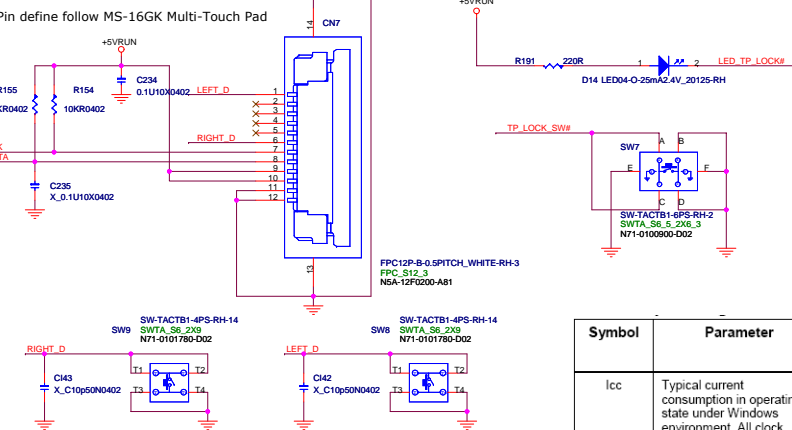


CAMERA LVDS ON



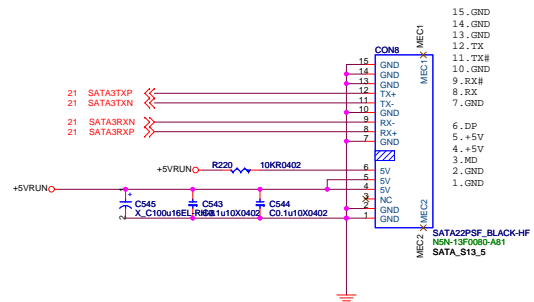


uch Pad

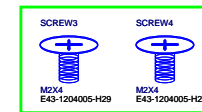
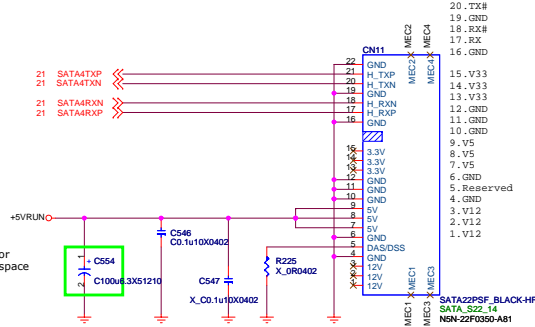


Symbol	Parameter	Limits	Unit
		Typ	
I _{CC}	Typical current consumption in operating state under Windows environment. All clock domains are running, and no keyboard/mouse activities.	20	mA

SATA ODD



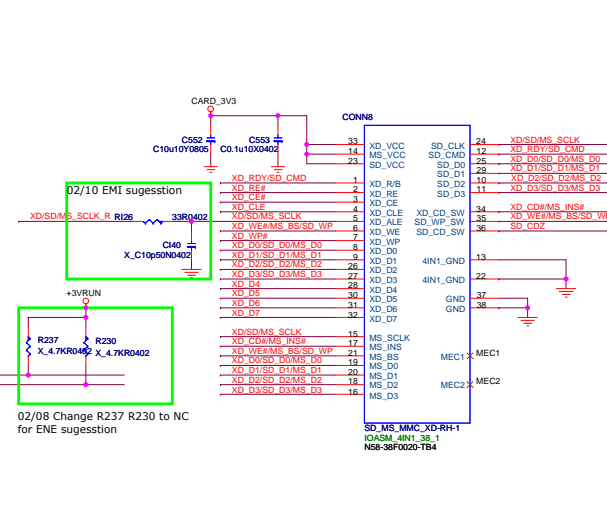
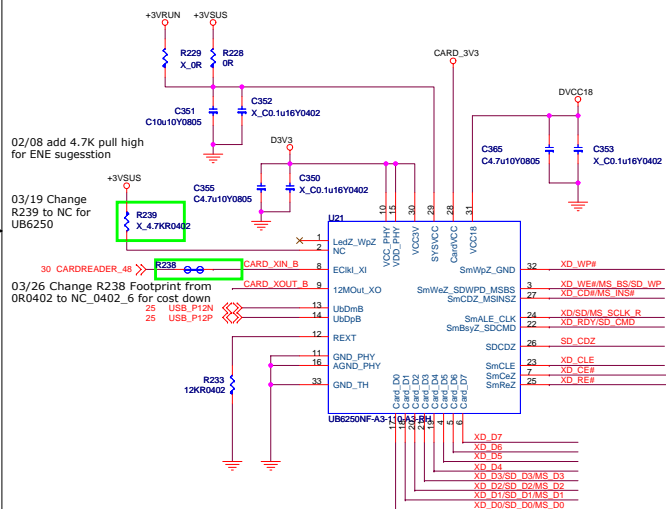
SATA HDD



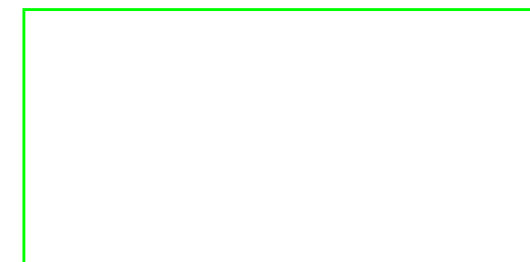
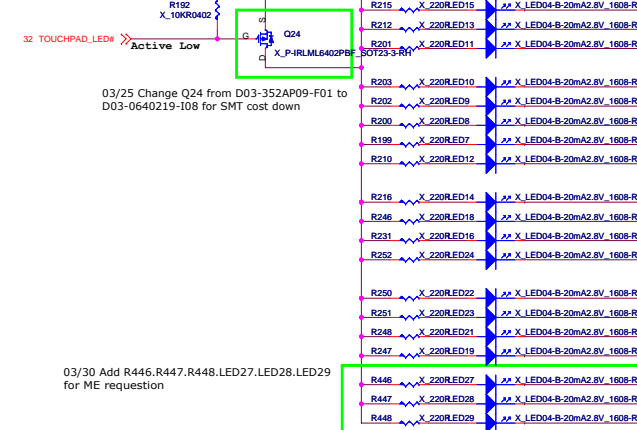
03/30 Add SCREW3, SCREW4 for ME request

02/02 Remove BT Connector

Card Reader UB6250

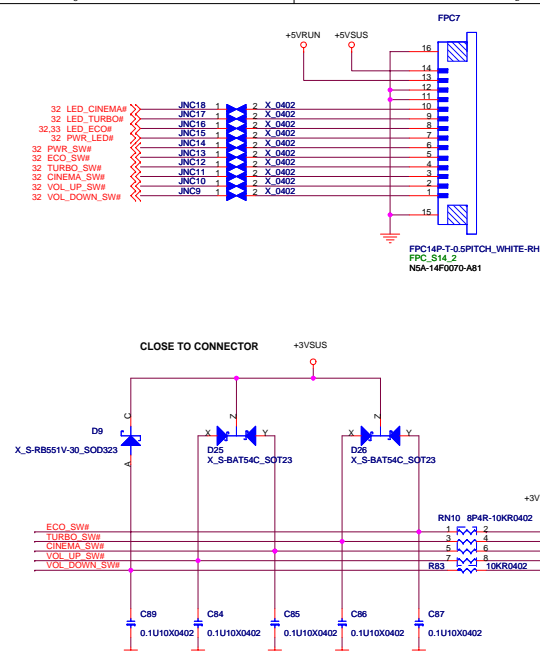
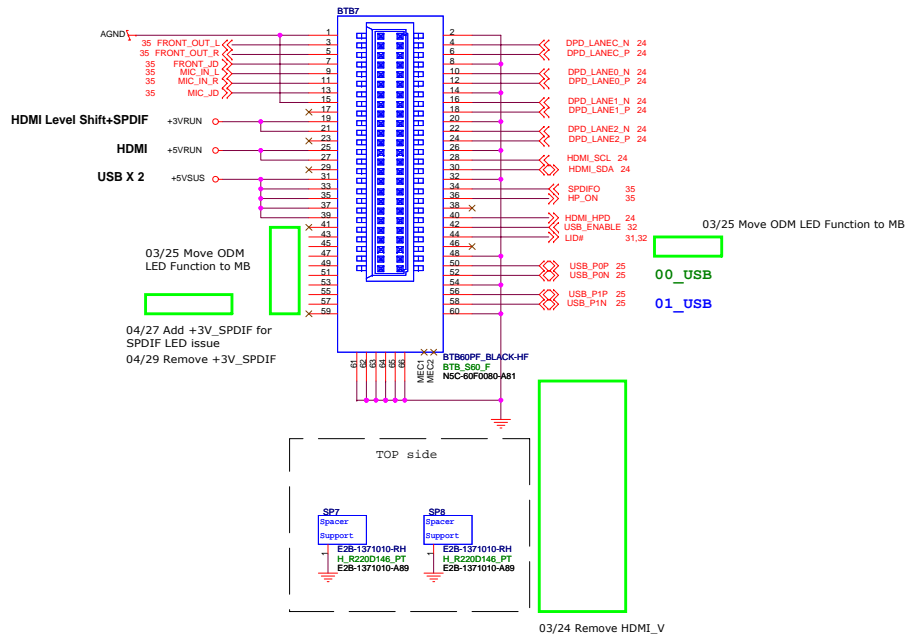


OEM TP LED

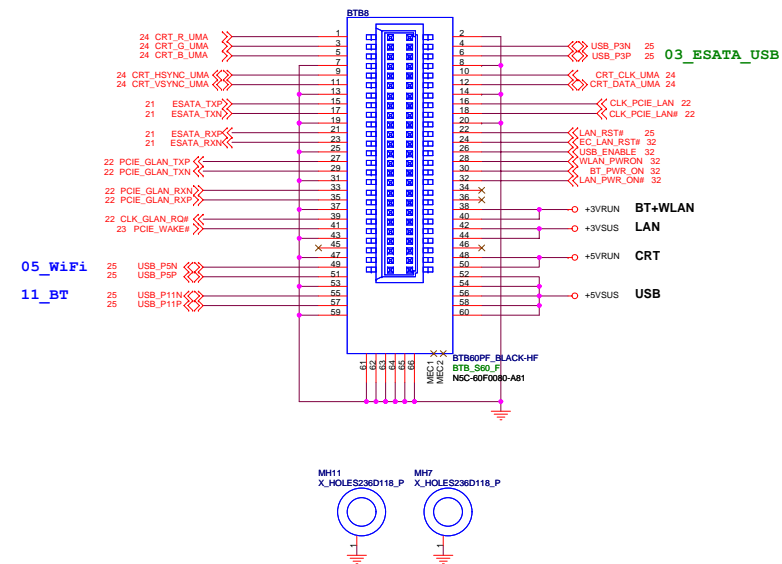


02/02 Remove LED for match Medion and Channel new rule

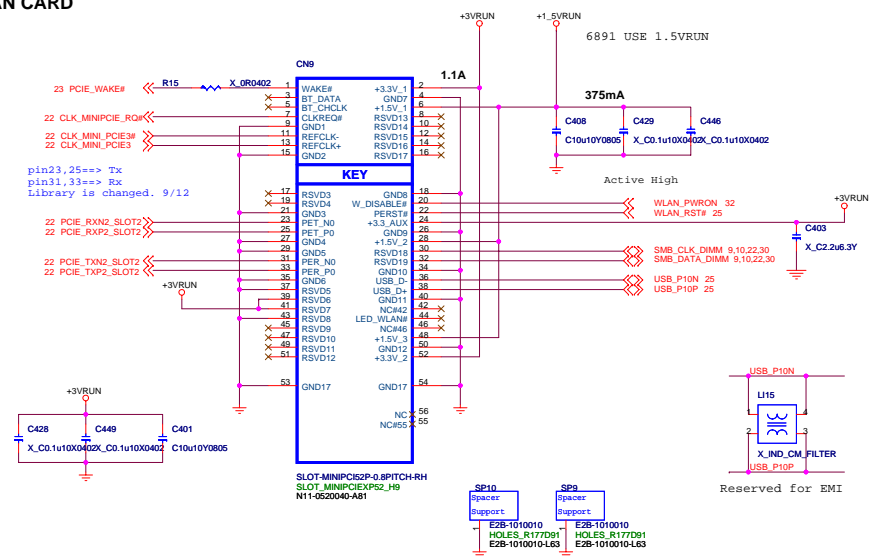
(才 凹HDMI,Audio,USB x 2)



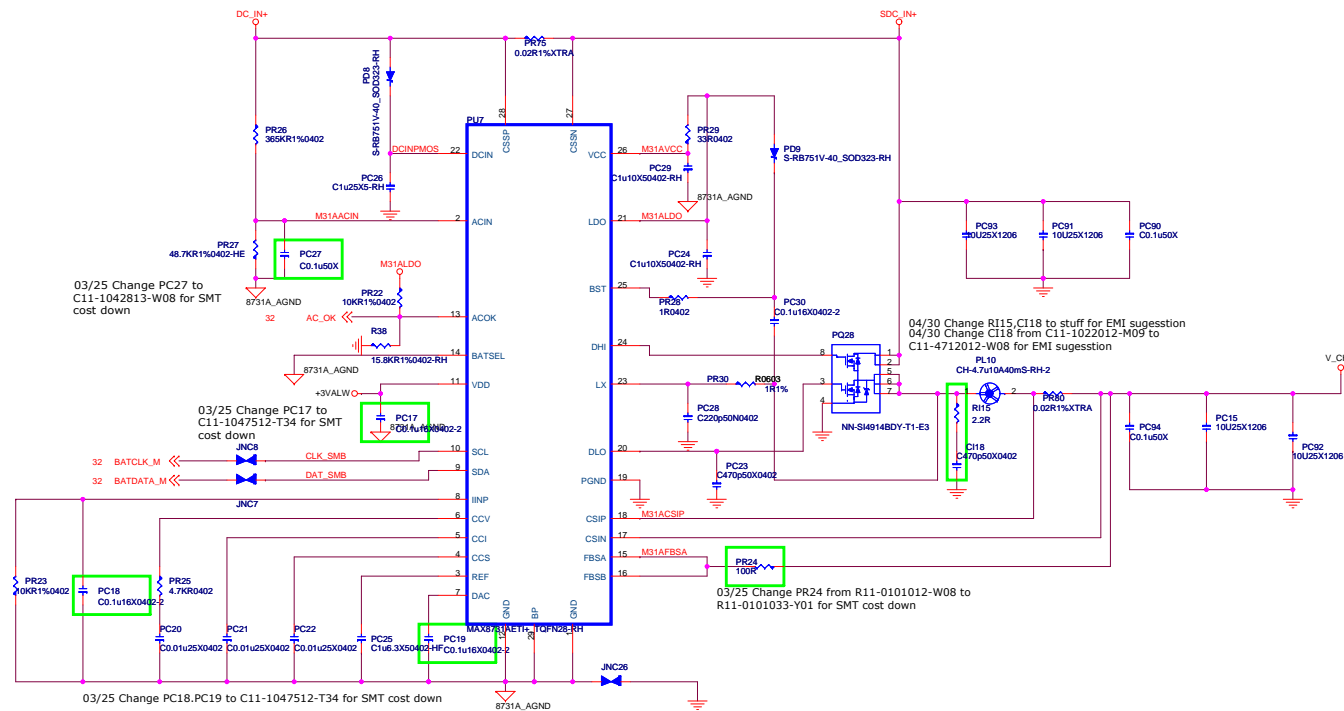
(㉔ESATA,USB,LAN,CRT,BT+WLAN)



WLAN CARD

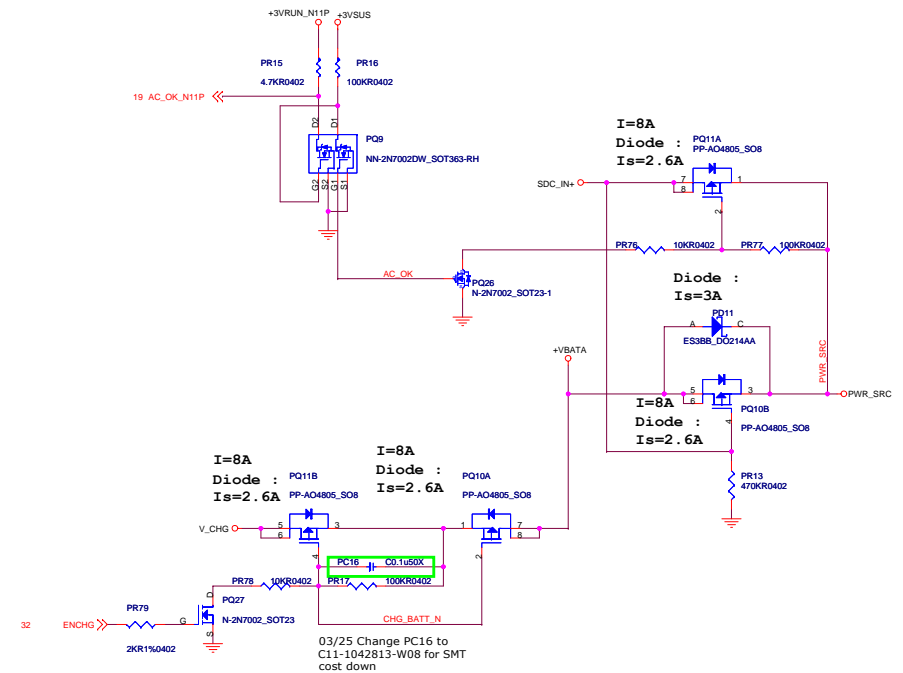
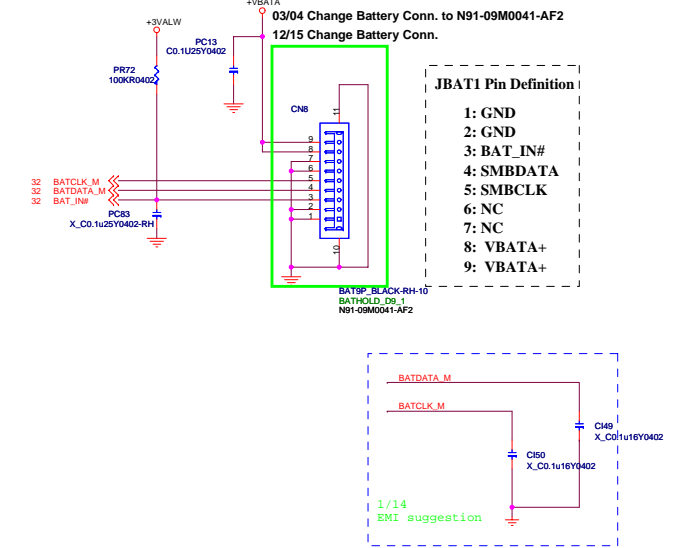
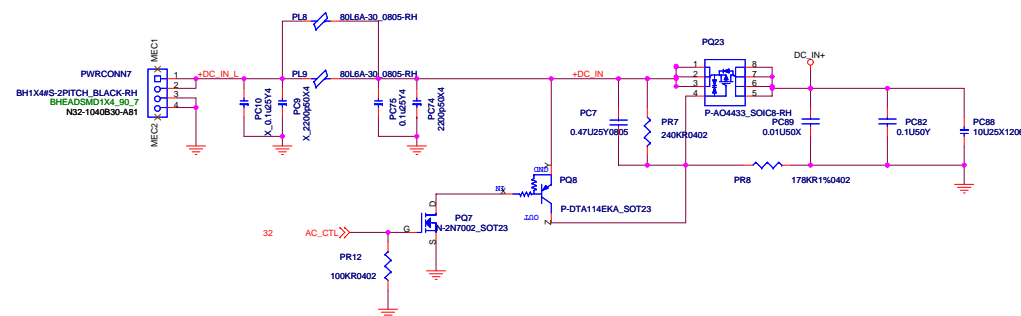


Adapter input voltage set 19 Voltage



IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP \times RS1 \times 3mA/V \times PR25$



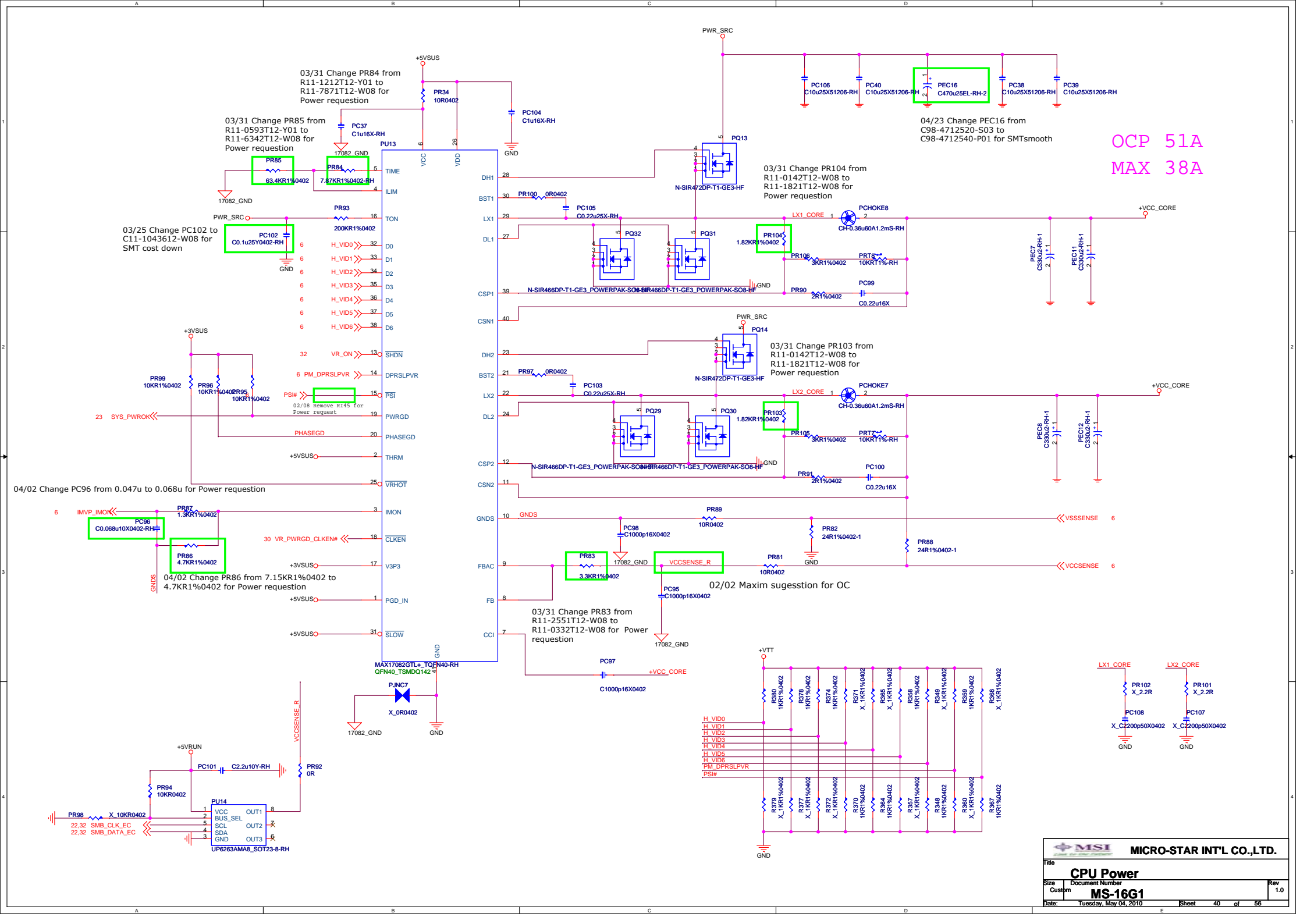
$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 1.82A$$

MAX 2A

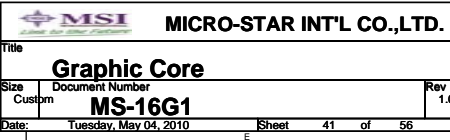
OCP 12A
MAX 8A

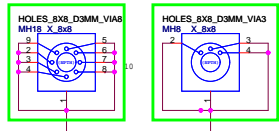
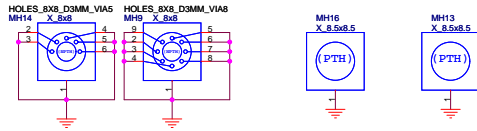
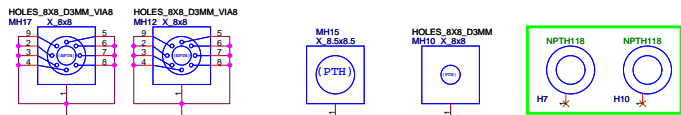
In current designs, Processor V_{DDQ} is powered with +V1.5, which is "ON" in S3. This is changed to a switching rail which is "OFF" during S3. A power FET is required to control the Processor V_{DDQ} (1.5 V) power. For N-FET (e.g., IRF7822 or RJK0346), gate voltage of FET (PS_S3CNTRL_1.5S) is derived from SLP_S3# and at 12-V logic. RDS(ON) of the FET used in CRB is in the range of 5 mΩ. Every design is different and designer should select an appropriate FET so that the required voltage rail specification is maintained at the Processor V_{DDQ} pins.

Signal Name	Source	Voltage Level	Comments
PS_S3CNTRL	Inverted SLP_S3# signal	In CRB, it is a 3.3-V signal.	Voltage should be high enough to turn ON or OFF the MOSFET. When selecting the MOSFET, insure $V_{gs} > V_{gsth}$.
PS_S3CNTRL_1.5S	Buffered SLP_S3# signal	In Intel CRB it is a 12-V signal.	Voltage should be high enough to turn ON or OFF the Power MOSFET. When selecting the MOSFET, insure $V_{gs} > V_{gsth}$.



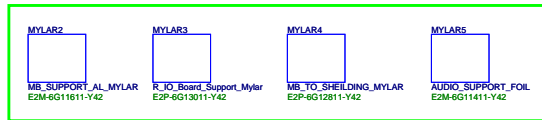
OCV 51A
MAX 38A



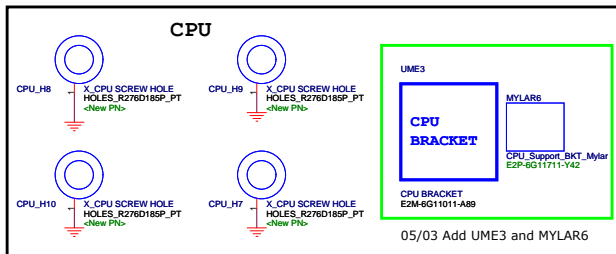


02/10 Change to 8 vias for EMI suggestion

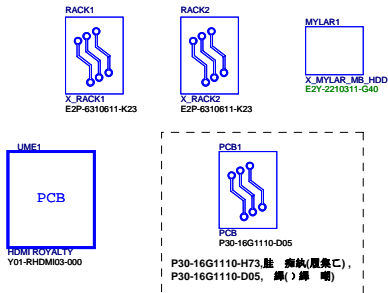
02/10 Add 3 vias for EMI suggestion



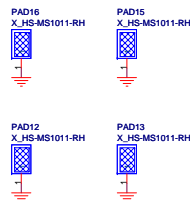
04/23 Add MYLAR2.MYLAR3.MYLAR4.MYLAR5 for ME request



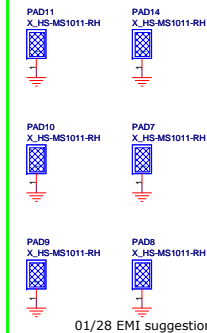
03/04 Change CPU Holes to NC



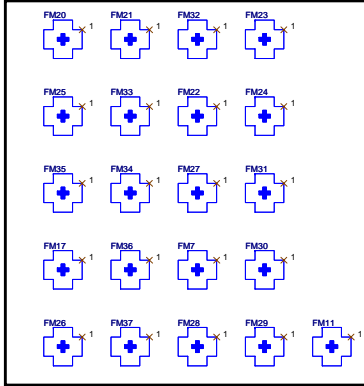
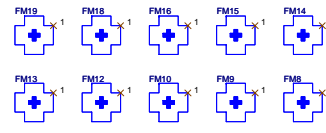
TOP SPRING



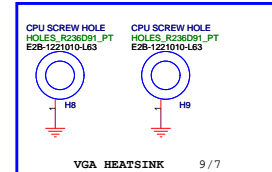
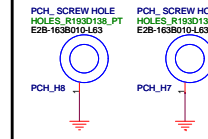
BOT SPRING



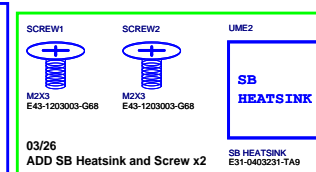
01/28 EMI suggestion



PCH

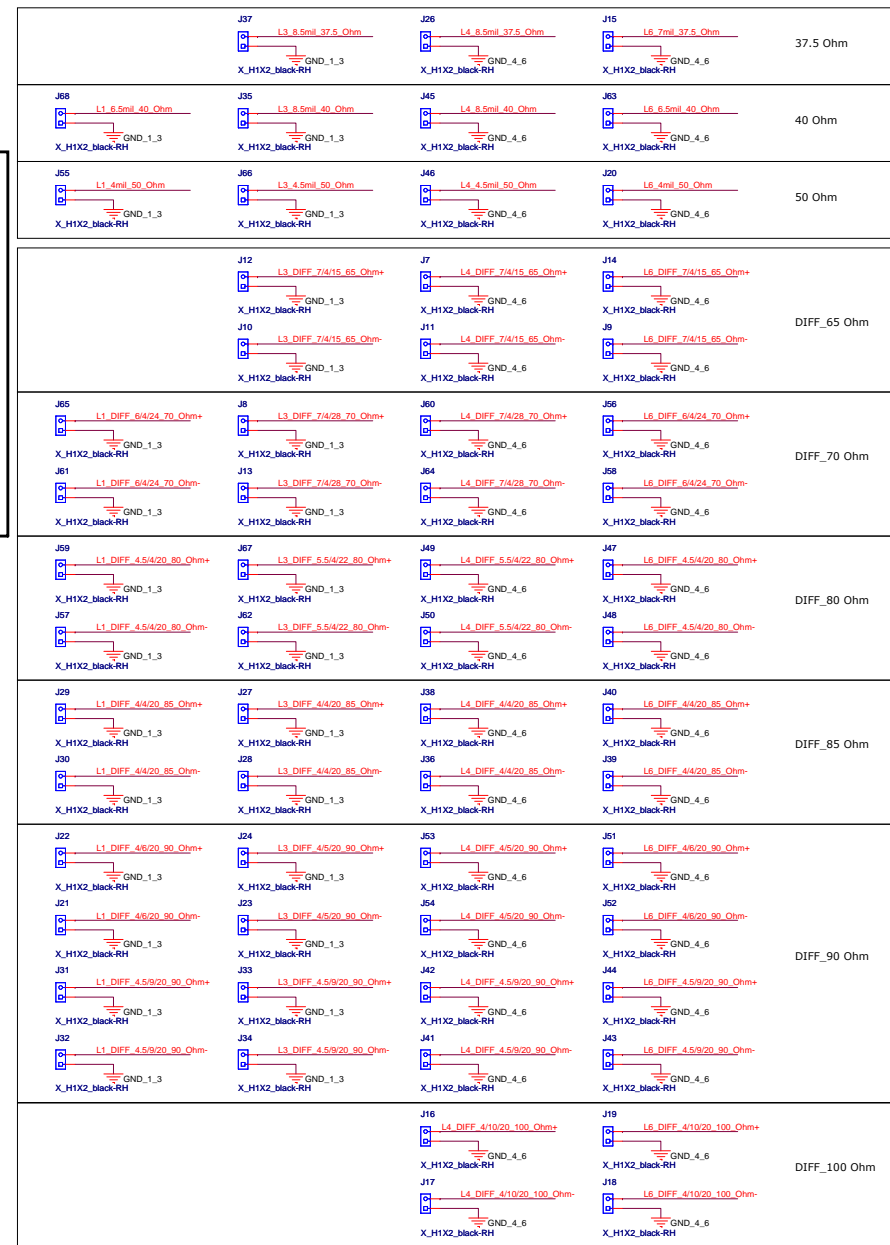


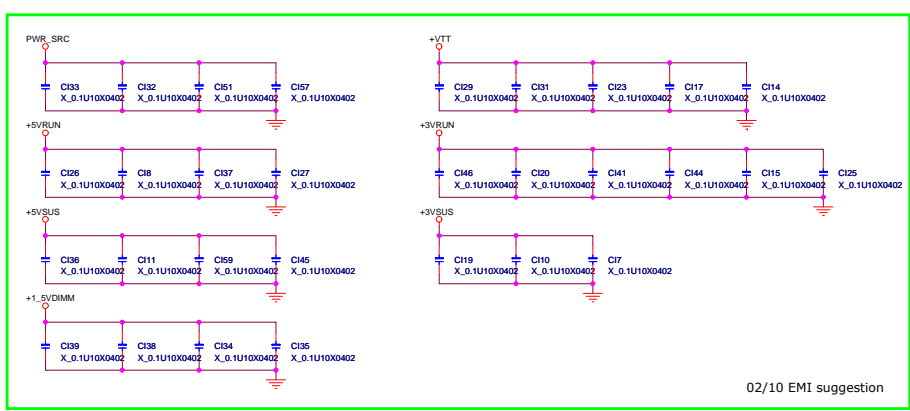
VGA HEATSINK 9 / 7



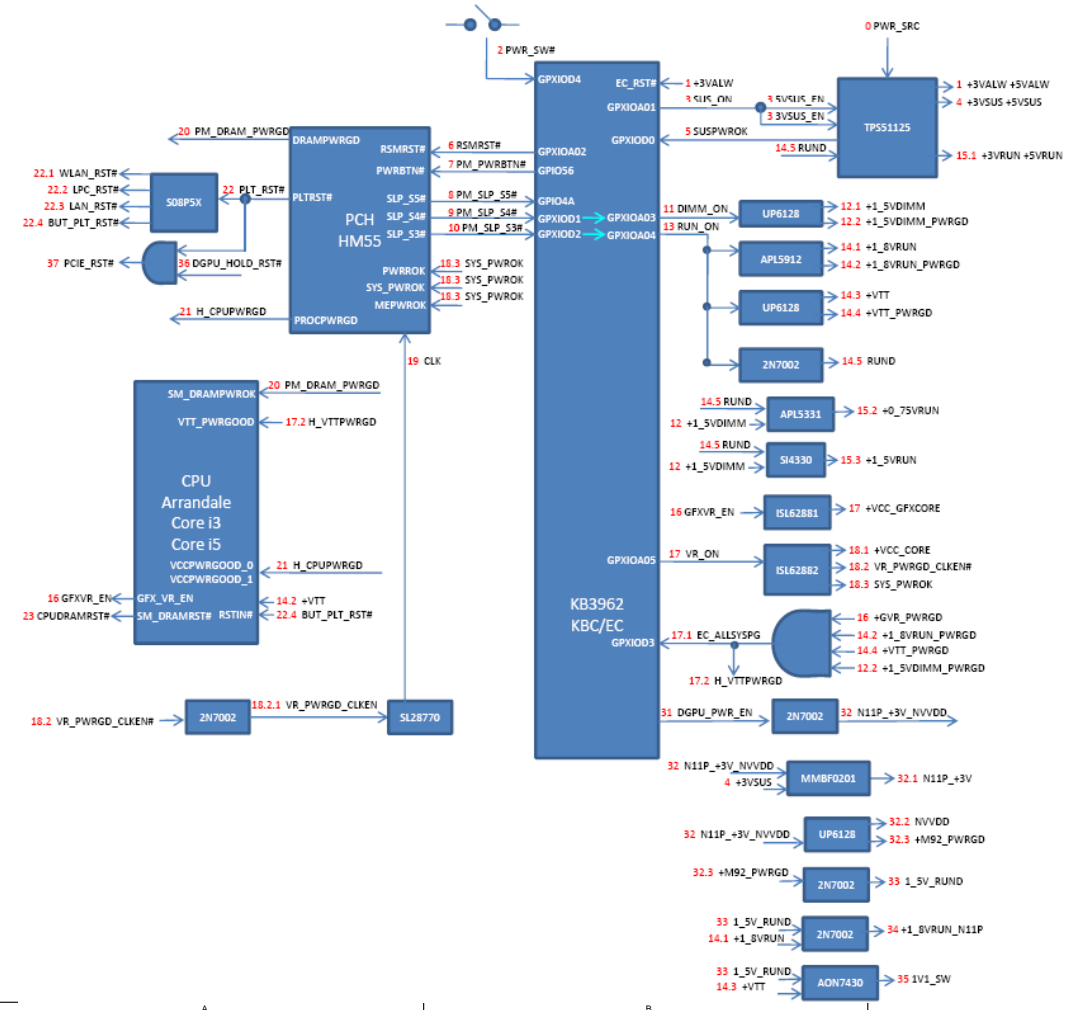
03/26 ADD SB Heatsink and Screw x2

SB HEATSINK E31-0403231-TA9

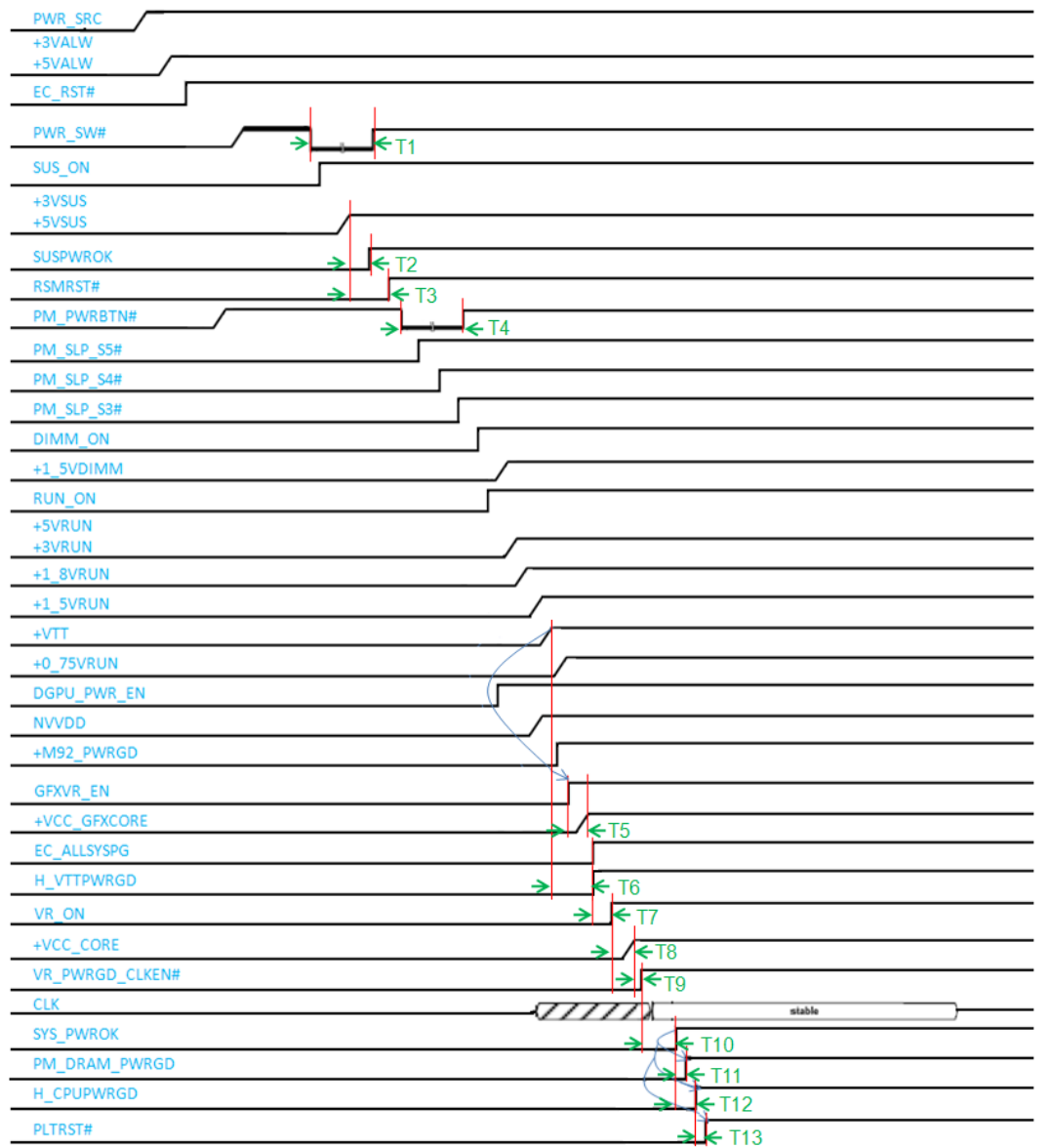




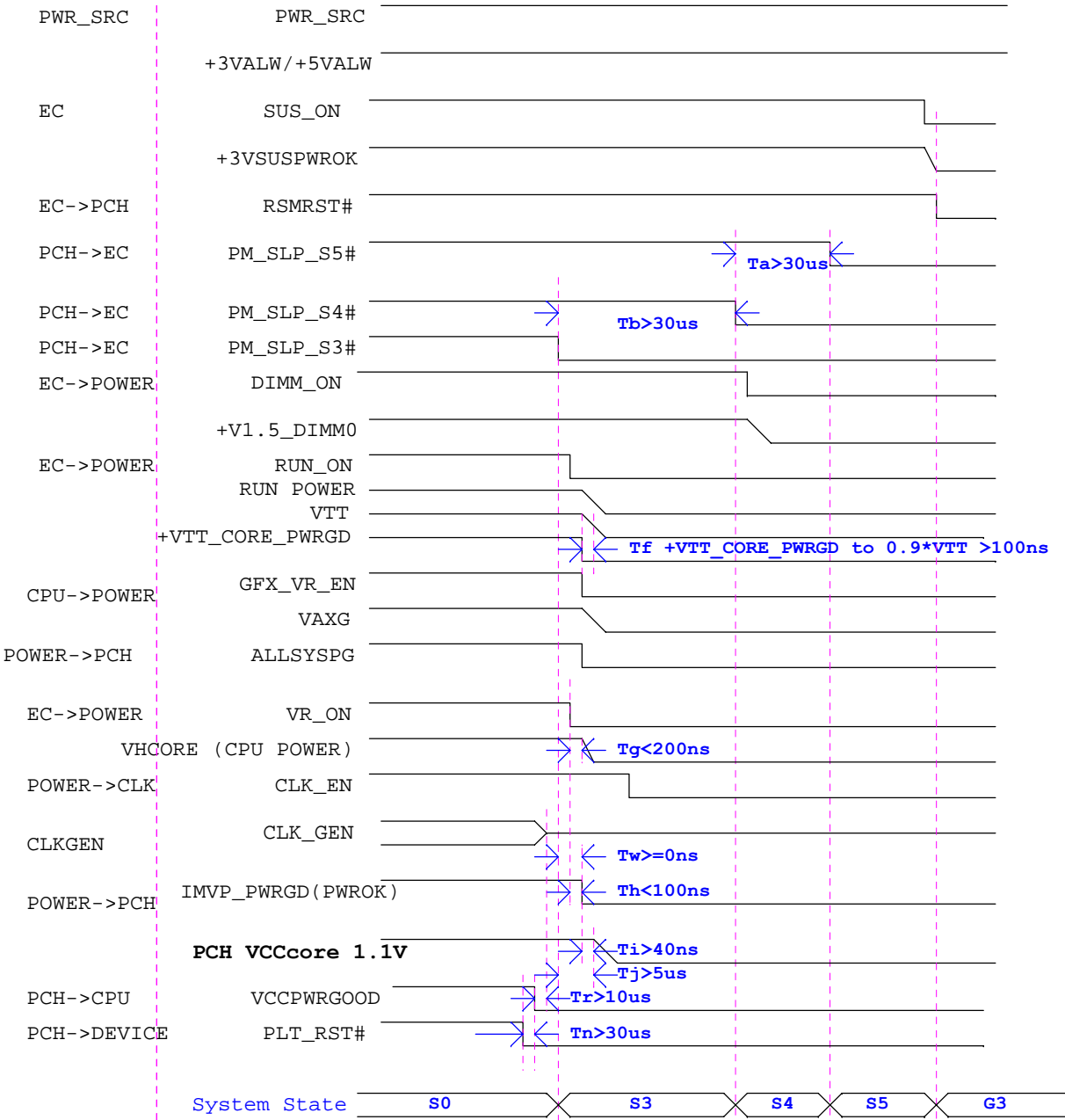
Label	Min	Max	Units	Description
T1	150		ms	
T2	2	2.5	ms	The powergood function is activated with 2 ms internal delay after SUSPWROK goes high. If the output voltage becomes within +/-5% of the target value, PGOOD goes high around 2.5 ms after SUSPWROK goes high.
T3	10		ms	Vcc_SUS stable to RSMRST# deassertion.
T4	150		ms	
T5		1	us	CPU will drive Gfx_VR_EN when VTT ramps. Gfx_VR_EN to Gfx_VID stable. Timing set by Processor.
T6		500	ms	VTT stable to VITTPWRGOOD assertion to the processor.
T7	99		ms	ALL_SYS_PWRGD assertion to IMVP_VR_EN. This timing is generated by EC.
T8		3	ms	
T9	10	100	us	
T10	3	20	ms	IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
T11	1		ms	SYS_PWROK/PCH_PWROK assertion to DRAMPWROK assertion. Timing set by PCH.
T12	1		ms	SYS_PWROK/PCH_PWROK assertion to VOCPPWRGOOD/VCCPWROK assertion. Timing set by PCH.
T13	1		ms	VCCPWROK assertion to PLTRST# deassertion.

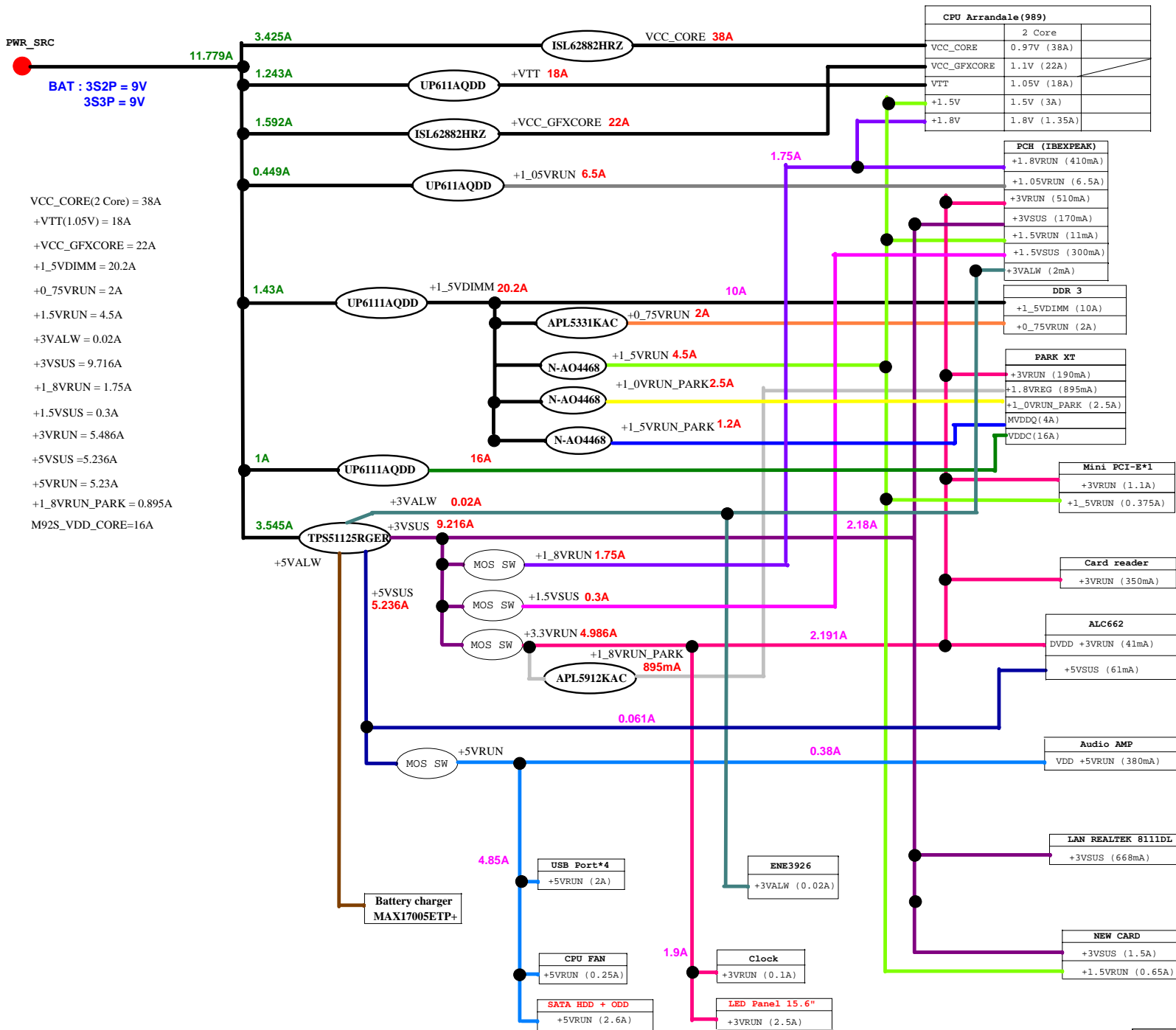


Calpella System Power on Sequence DC mode

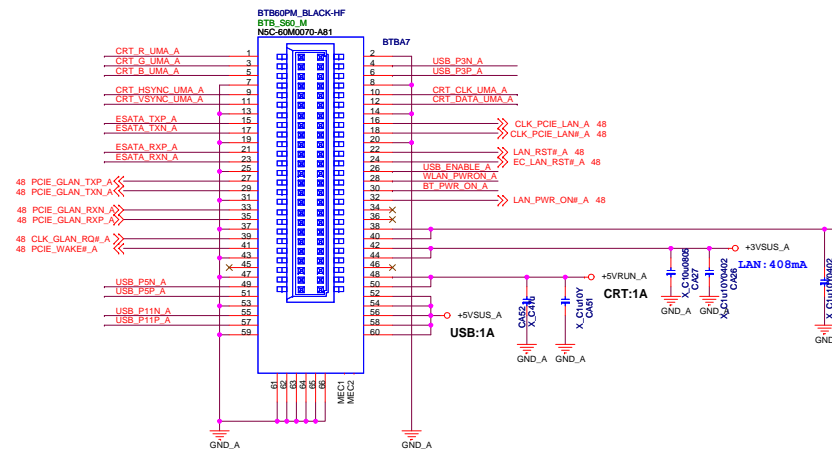


Power down Sequence DC mode S0 to G3





(凹)ESATA,USB,LAN,CRT,BT+BT+WLAN)



02/25 Change MHA8 to HOLES_R276D185P_PT

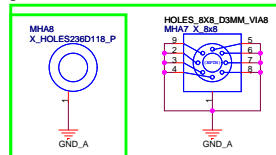
03/30 Change MHA8 to HOLES236D118_P

PCBA1

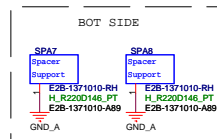
PCB

PCB_V10

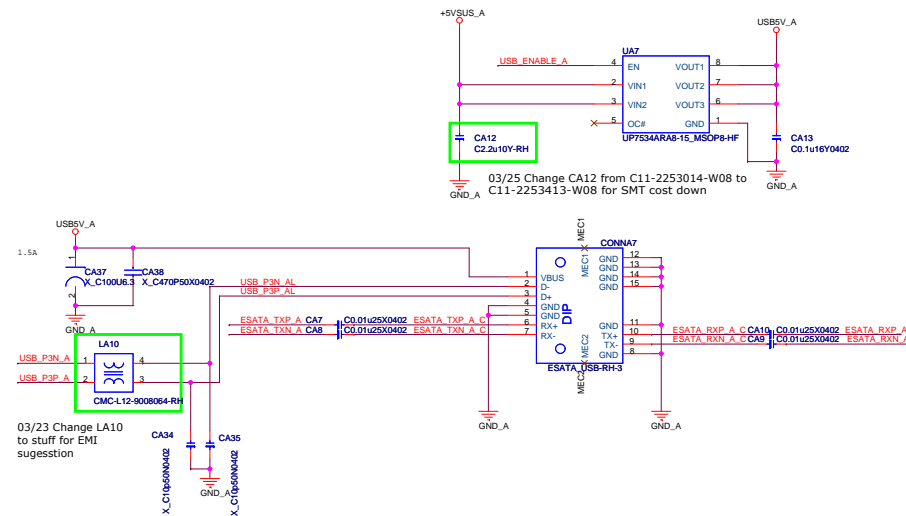
P30-16G1A10-D05



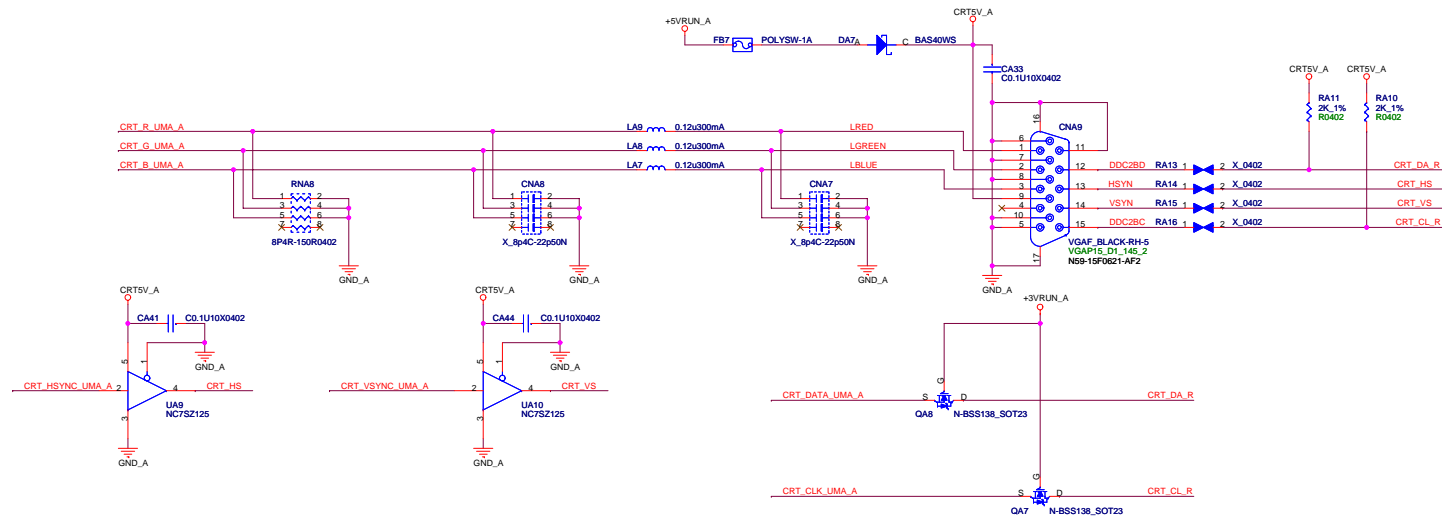
02/23 Change to 8 vias for EMI suggestion



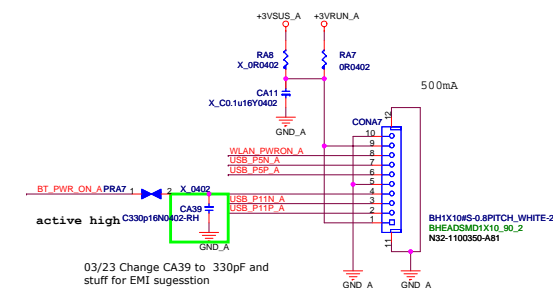
ESATA Connector

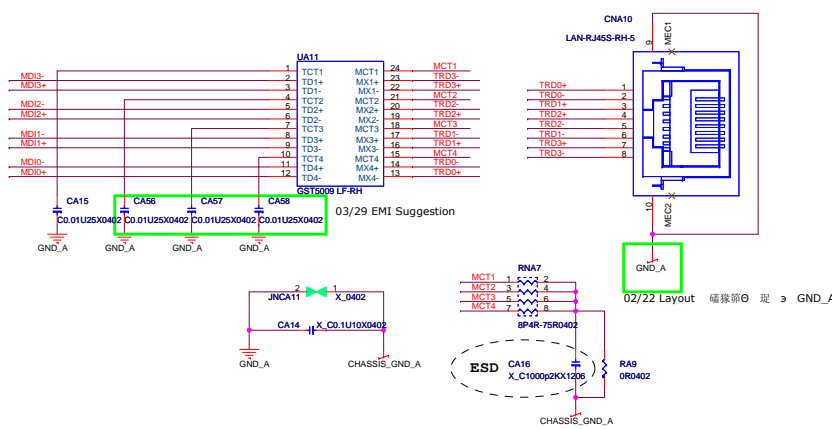
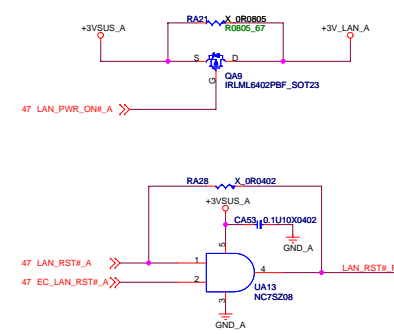
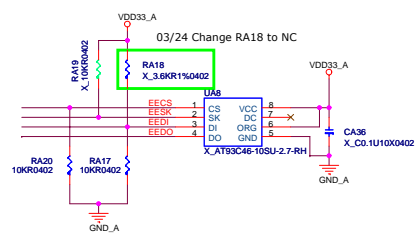
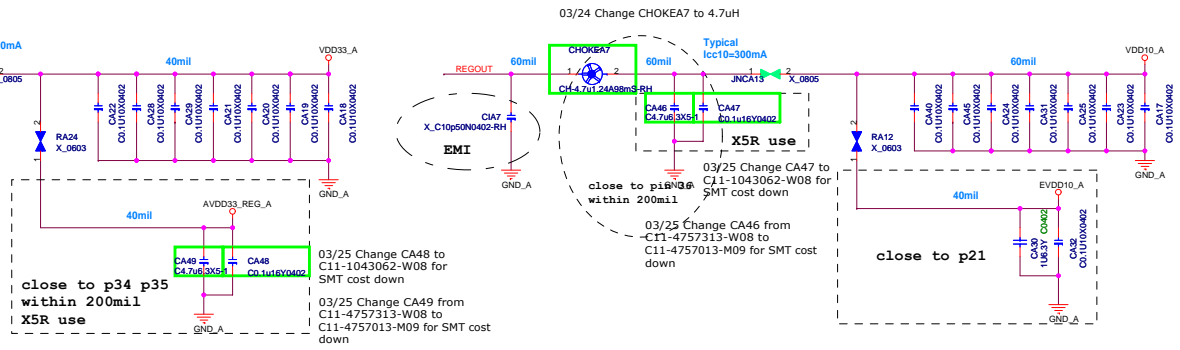
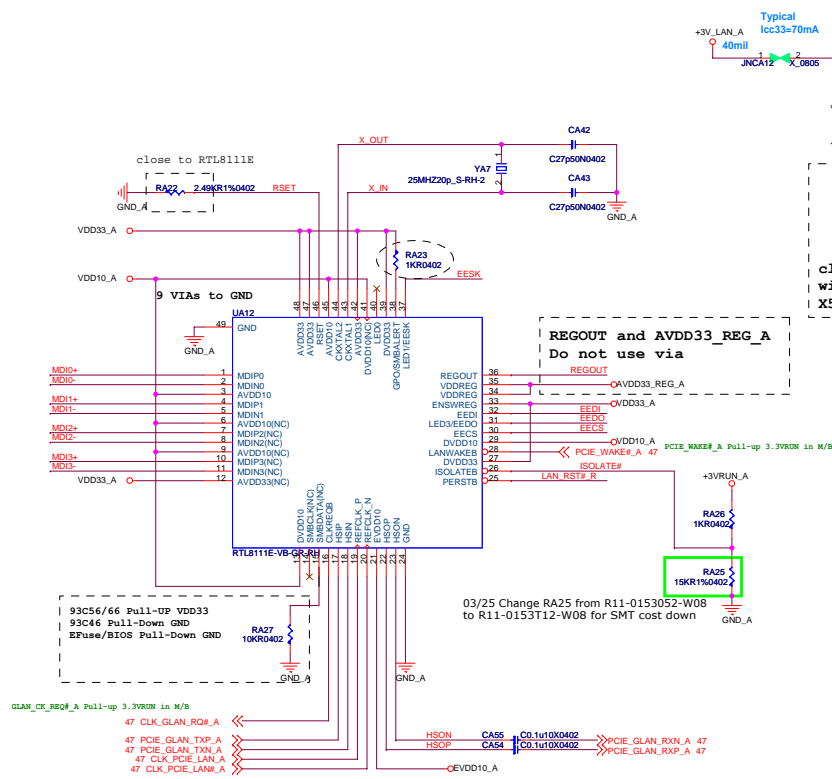


D-Sub Connector

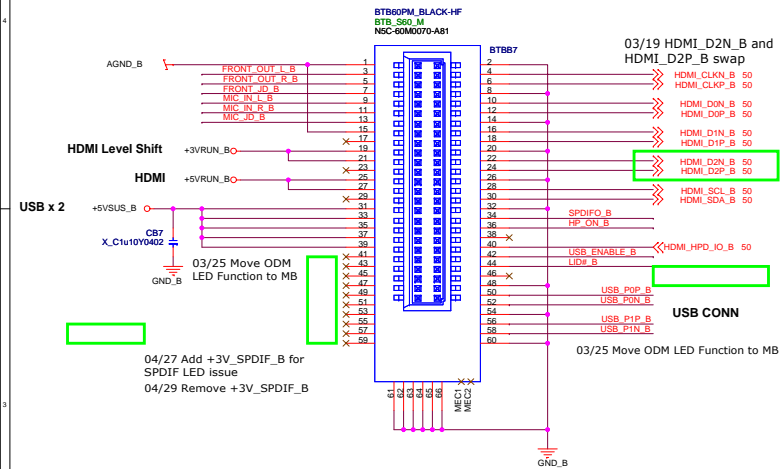


BT and WLAN Combo Connector

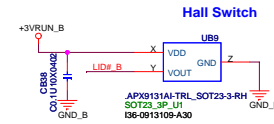




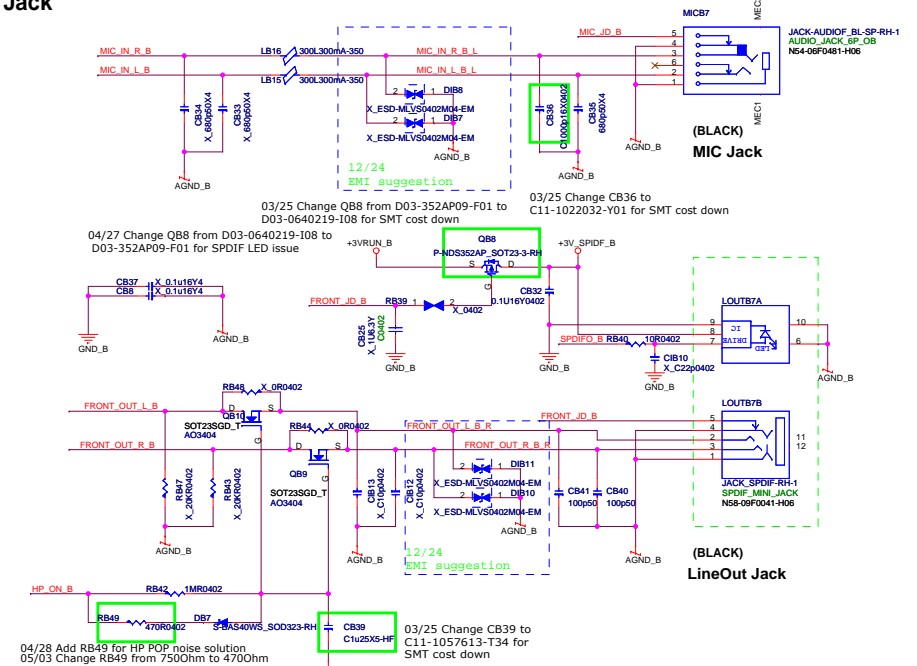
(才 凹HDMI,Audio,USB x 2)



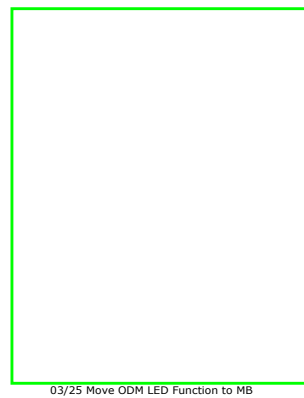
LID Switch



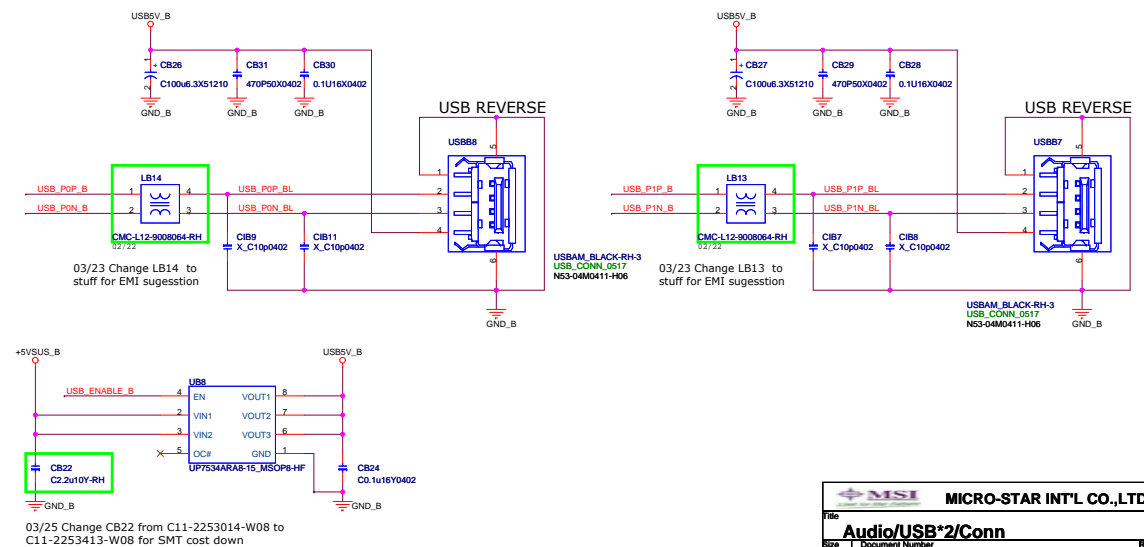
Audio Jack



For ODM LED Function



USB 2.0 Connector



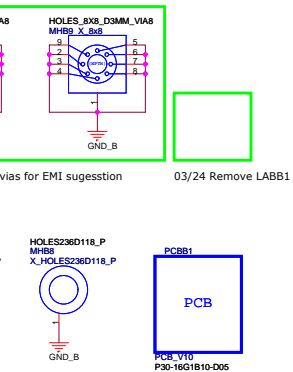
03/25 Change RB45 and
to R11-0202T12-W08

HP_DET

OE#

UNPLUG 0 1 (HIGH Z)

PLUG 1 0 (ACTIVE)



03/24 Remove LABB1

PCB

04/30 Change RIB7,RIB8,RIB9,CB23 from R11-0181012-W08 to R11-0331012-W08 and stuff on for EMI suggestion

Q20212-W08

W01

+5VRUN_B

HDMI D2P R_B
HDMI D2N R_B

HDMI D1P R_B
HDMI D1N R_B

HDMI D0P R_B
HDMI D0N R_B

HDMI CKLP R_B
HDMI CKLN R_B

HDMI SCL R
HDMI SDA R

FB8

POLYSW-1A

HPD HDMI IO R

+5VRUN_B

+5VRUN_B

0D8

BAV99LT1_S073

GND_B

CLOSE TO CONNECTOR

CNB7

SHELL1

D2+
D2- Shield/GND
D2-
D1+
D1- Shield
D0- Shield
D0-
CK+
CK-
CK Remote
CE
CLCK
CLNK
SCL
NC
D0 CLK
D0 GND
D0 DATA
+5V
HP DET
SHELL2

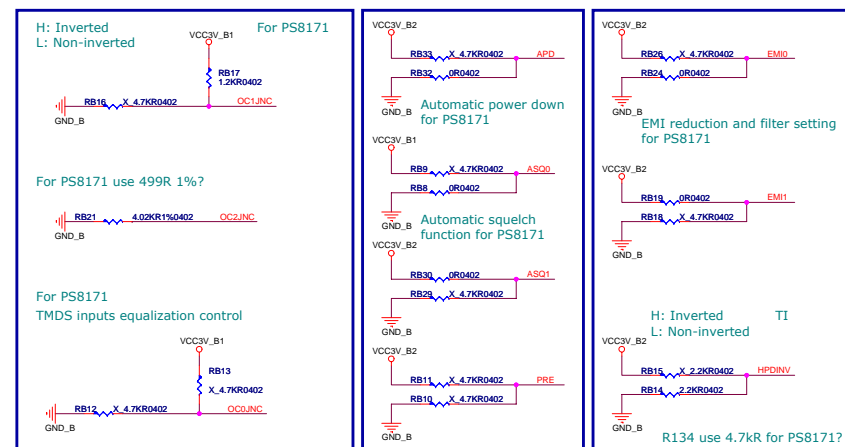
20
22
MEC2
MEC1

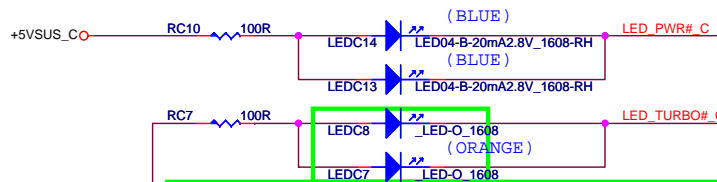
23
21

CONN+HDMI19P BLACK-RH-4
HDMI S10 3
HDMI-19M010-8P-2



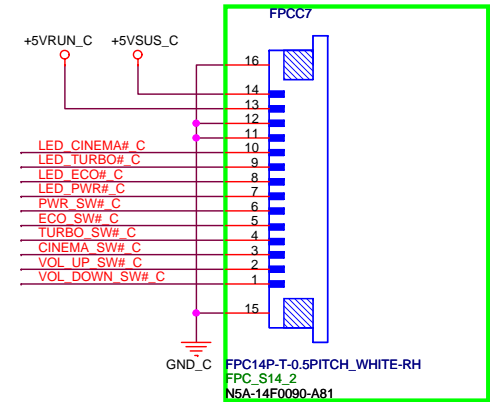
Note2: High is HPD logic inverted, Low is HPD logic non-inverted



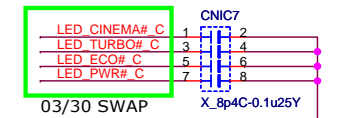
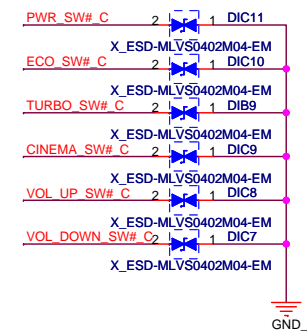
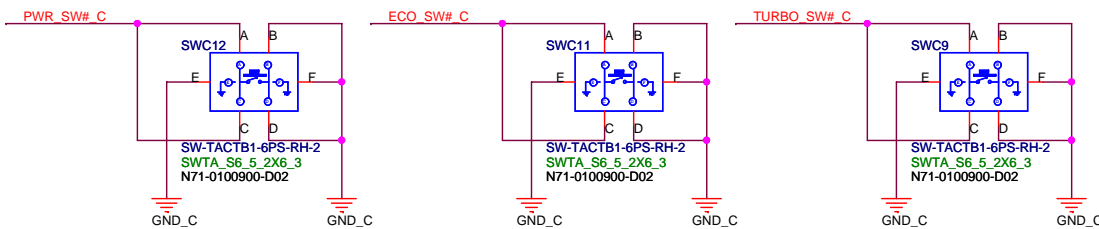


03/30 Change LEDC7.LEDC8 from D0C-04018F0-L05 to D0C-0400600-E07

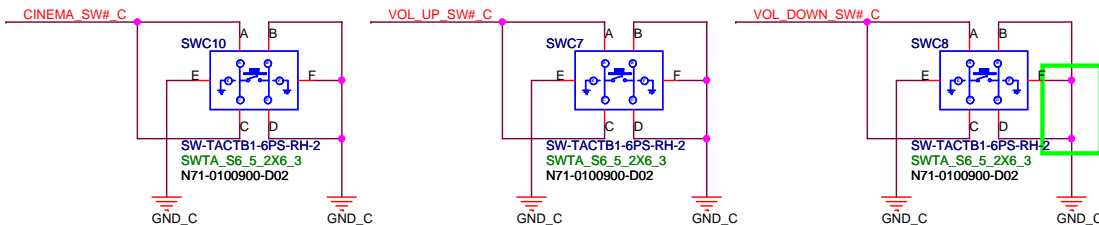
03/29 Remove ECO and Cinema LED for ID request



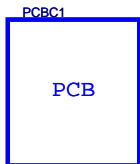
04/23 Change FPCC7 from N5A-14F0070-A81 to N5A-14F0090-A81(P/N only) for ME request



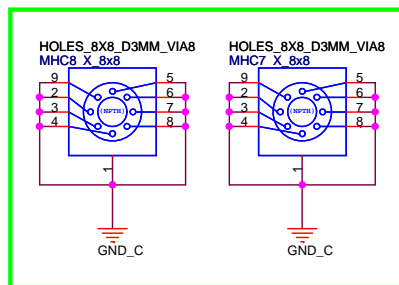
03/30 SWAP



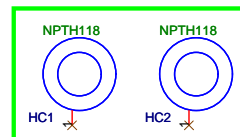
04/28 Fix SWC8's HW mismatch



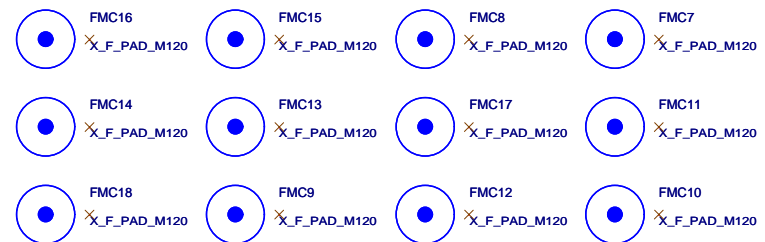
PCB_V10
P30-16G1C10-D05



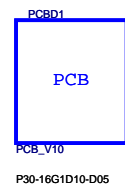
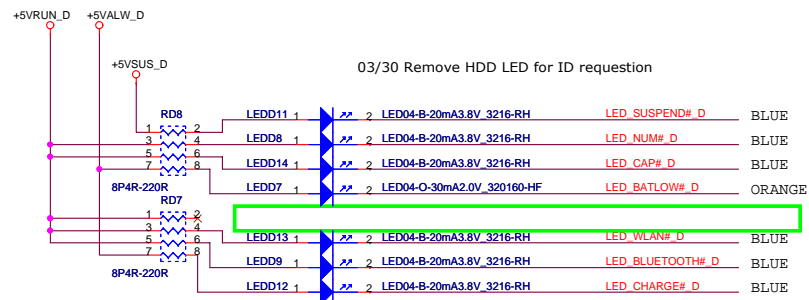
02/10 Add 8 vias for EMI suggestion



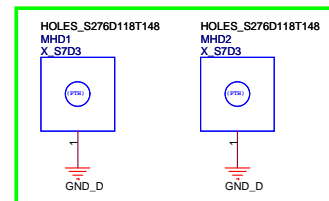
03/26 Add ME



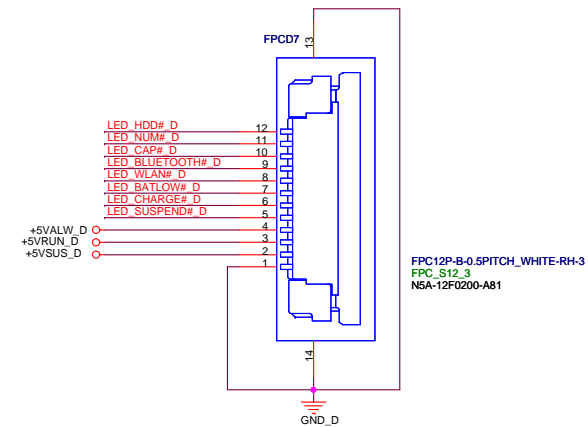
MSI Link for Your Solution		MICRO-STAR INT'L CO.,LTD.	
Title PWR SW / LED			
Size B	Document Number MS-16G1C		Rev 0A
Date:	Sheet 51		of 56

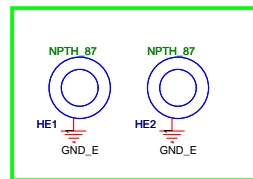
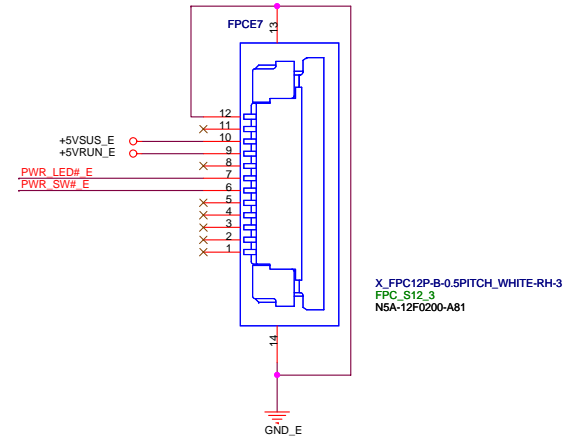
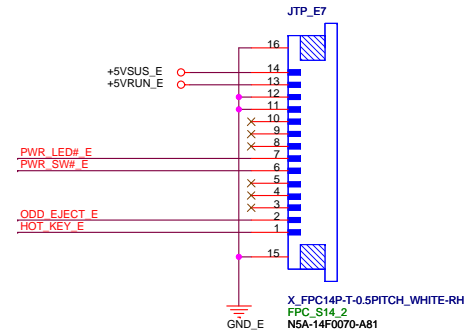
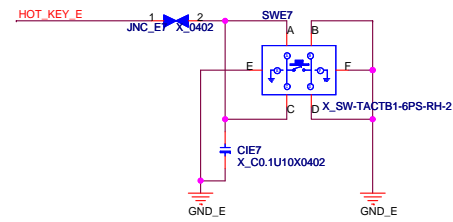
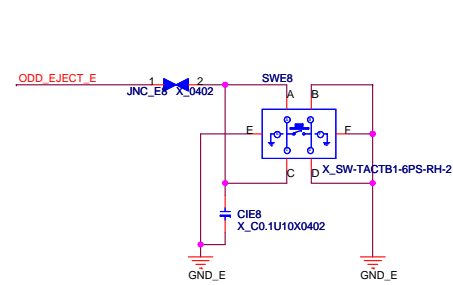


03/30 Add MHD1 and MHD2 for ME request

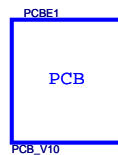


02/10 Reverse Swap Pin define

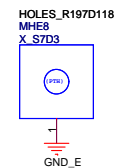
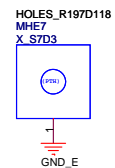


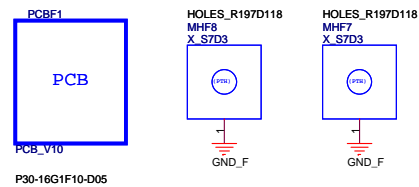


04/30 Add HE1,HE2 for ME request



P30-16G1E10-D05





A		C		D		E	
O.A		O.B					
2010/03/04	Change D21.D23 to D0C-04018F0-L05 and footprint change to LEDS_19_21SYGC	2010/03/25	Change D7 and D8 from D01-RB551V0-R06 to D01-BAS4000-W01 for SMT cost down Change PR24 from R11-0101012-W08 to R11-0101033-Y01 for SMT cost down Change R91 from R11-0103033-Y01 to R11-0103012-Y01 for SMT cost down Change R164,R167,R168,R169 from R11-0104043-W08 to R11-0104042-W08 for SMT cost down Change RA25 from R11-0153052-W08 to R11-0153T12-W08 for SMT cost down Change RB45 and RB46 from R11-0202012-W08 to R11-0202T12-W08 for SMT cost down Change R331 from R11-0560012-C36 to R11-0560T12-W08 for SMT cost down Change R335 from R11-0822T12-Y01 to R11-0822012-R01 for SMT cost down Change R345 from R11-0822T13-Y01 to R11-0822012-R01 for SMT cost down Move ODM LED Function from B Daughter Board to MB				
2010/03/19	Change R123 to 40.2R 1% for N11P-GV1 spec. Change R63.R75 to 40.2KR 1% for N11P-GV1 spec. Change U21 to UB6250 Change R239 to NC for UB6250 Change PR67 to 4.22KR 1% for Power requestion Change PR65 to 2KR 1% for Optimus function stable Change PC12 to stuff for Power requestion HDMI_D2N_B and HDMI_D2P_B swap	2010/03/26	Add ME ㄟ ㄟ Change R428,R410,R402,R320,R322,R41,R39,R30,R90,R307,R238,R401,RB23 Footprint from 0R0402 to NC_0402_6 for cost down ADD SB Heatsink and Screw x2				
O.B		2010/03/29	Add ECO LED for Medion Add CA56~CA58 for EMI Suggestion Remove ECO and Cinema LED for ID requestion				
2010/03/23	Change C346.C376 to 10uF and stuff Change C347.C375 to stuff Add R443 for FSA pull high resister Move LID# pull high resister R444 to Main board Change R166.R165 stuff states for mute AMP pop noise Add C555.C556 for system stable Change CA39 to 330pF and stuff for EMI sugesstion Change LA10.LB13.LB14 to stuff for EMI sugesstion Keyboard pin define swap	2010/03/30	Change MHA8 to HOLES236D118_P Add MHD1 and MHD2 for ME requestion Change D21 from D0C-0403000-E07 to D0C-0400600-E07 Change LEDC7.LEDC8 from D0C-04018F0-L05 to D0C-0400600-E07 Add R446.R447.R448.LED27.LED28.LED29 for ME requestion Remove HDD LED for ID requestion Add SCREW3.SCREW4 for ME requestion				
2010/03/24	Change C65.C68.C80.C443.R76 to NC Copy BIOS1 info. to SPI_SOCKET7 and remove BIOS1 Remove HDMI_V and LABB1 Change RA18 to NC Change CHOKEA7 to 4.7uH Change C346.C347.C375.C376 to NC Change R221 to 1KR	2010/03/31	Change PR61 from R11-3651T12-C36 to R11-0222T12-W08 for Power requestion Change PR85 from R11-0593T12-Y01 to R11-6342T12-W08 for Power requestion Change PR84 from R11-1212T12-Y01 to R11-7871T12-W08 for Power requestion Change PR83 from R11-2551T12-W08 to R11-0332T12-W08 for Power requestion Change PR103.PR104 from R11-0142T12-W08 to R11-1821T12-W08 for Power requestion				
2010/03/25	Change PC117 to C11-1011512-W08 for SMT cost down Change CI21.CI22 to C11-1012012-W08 for SMT cost down Change C502.C503.C504.C505.CB36 to C11-1022032-Y01 for SMT cost down Change C11.C29.C394 to C11-1032082-W08 for SMT cost down Change C16.C30.C31 to C11-1032082-W08 for SMT cost down Change PC16.PC27 to C11-1042813-W08 for SMT cost down Change PC61.PC71.PC78.PC102.PC127 to C11-1043612-W08 for SMT cost down Change C7.C335.CA47.CA48 to C11-1043062-W08 for SMT cost down Change PC17.PC18.PC19 to C11-1047512-T34 for SMT cost down Change C24.C192.C218.C222.C416.C452.C479.C481 to C11-1042042-W08 for SMT cost down Change C442 to C11-1053312-W08 for SMT cost down Change CB39 to C11-1057613-T34 for SMT cost down Change C308.C322 from C11-1067313-T04 to C11-1067014-T04 for SMT cost down Change C12.C337.C402.C431 from C11-1067314-T34 to C11-1067014-T04 for SMT cost down Change C95.C109 from C11-106A334-S02 to C11-1067014-T04 for SMT cost down Change C38.C166 from C11-2242033-S02 to C11-2242013-W08 for SMT cost down Change C200.C202 from C11-2253013-Y01 to C11-2253413-W08 for SMT cost down Change CA12.CB22 from C11-2253014-W08 to C11-2253413-W08 for SMT cost down Change C287.C298.C301 from C11-2257423-T34 to C11-2253413-W08 for SMT cost down Change C8 from C11-2263027-W08 to C11-2267014-M09 for SMT cost down Change C99.C121 from C11-2267334-A15 to C11-2267014-M09 for SMT cost down Change C19.PC62.PC63 from C11-2267367-M09 to C11-2267014-M09 for SMT cost down Change PC33 from C11-4712522-W08 to C11-4712012-W08 for SMT cost down Change C537 from C11-4732012-W08 to C11-4732412-W08 for SMT cost down Change PC45 from C11-4757014-W08 to C11-4757013-M09 for SMT cost down Change CA46.CA49 from C11-4757313-W08 to C11-4757013-M09 for SMT cost down Change C237.C238.C277.C278.C279.C281 from C11-4757434-T34 to C11-4757013-M09 for SMT cost down Remove Power Gap G7.G8.G9.G10.G11.G13.G14 Change QB8 from D03-352AP09-F01 to D03-0640219-I08 for SMT cost down Change Q24 from D03-352AP09-F01 to D03-0640219-I08 for SMT cost down	2010/04/02	Change PC96 from 0.047u to 0.068u for Power requestion Change PR86 from 7.15KR1%0402 to 4.7KR1%0402 for Power requestion				
		2010/04/08	Change C347 and C375 to stuff for SA debug				
		1.O					
		2010/04/23	Add MYLAR2,MYLAR3,MYLAR4,MYLAR5 for ME request Change PEC16 from C98-4712520-S03 to C98-4712540-P01 for SMT smooth Change FPCC7 from N5A-14F0070-A81 to N5A-14F0090-A81(P/N only) for ME request				
		2010/04/27	Remove R163 Fix incorrect circuit @ P35 Add R449.Q33.Q34.+3V_SPDIF for SPDIF LED issue Change QB8 from D03-0640219-I08 to D03-352AP09-F01 for SPDIF LED issue Change Gpu Footprint from BGA969_1 to BGA973 for description incorrect				
		2010/04/28	Change CONN7 to NC for MVT Change Q20.S1 input from PD# to EAPD for HP POP noise solution Change R449 from 10kOhm to 100kOhm Change Q21.S1 input from CODEC_HDA_RST# to EC_MUTE# for HP POP noise solution				
		<div><div><div><div><div><div></div><div>MICRO-STAR INT'L CO.,LTD.</div></div></div><div><div><div>Title</div><div>History</div></div><div><div>Size</div><div>Document Number</div><div>Rev</div></div><div><div>Custom</div><div>MS-16G1</div><div>0A</div></div><div><div>Date</div><div>Friday, April 30, 2010</div><div>Sheet</div><div>55</div><div>of</div><div>56</div></div></div></div></div></div>					

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2010/04/28 Add R451
Add R450 for HP POP noise solution
Add RB49 for HP POP noise solution
Change R184 to NC for ACPI POP noise issue and Realtek suggestion
Change Q21.S1 input from CODEC_HDA_RST# to EC_MUTE# for HP POP noise solution
Change Q20.S1 input from PD# to EAPD for HP POP noise solution
Change R175.R174.Q21 to NC for HP POP noise sulation
Change Q20,Q21 from BSS138 to 2N7002
Change R449 from 10kOhm to 100kOhm
Change C495 from C11-1067038-T34 to C11-1053054-W08
Change R170 from 100kOhm to 33kOhm
Fix SWC8's HW mismatch


2010/04/29 Remove R449.Q33.Q34.+3V_SPDIF

2010/04/30 Change RI15,CI18 to stuff for EMI suggestion
Change CI18 from C11-1022012-M09 to C11-4712012-W08 for EMI suggestion
Add CI60,CI60,CI62,CI63,CI64 for EMI suggestion
Change CI12,CI13,CI9 from to C11-1001012-W08 and stuff on for EMI suggestion
Change RIB7,RIB8,RIB9,CB23 from R11-0181012-W08 to R11-0331012-W08 and stuff on for EMI suggestion
Add HE1,HE2 for ME requeston

2010/05/03 Add UME3 and MYLAR6
Change RB49 from 750Ohm to 470Ohm

2010/05/04 Change PR10,PR41,PR141,PC8,PC50,PC131 to stuff for Power requeston

2010/05/11 Change PR59 from 10.7K to 11.3K for system stable



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